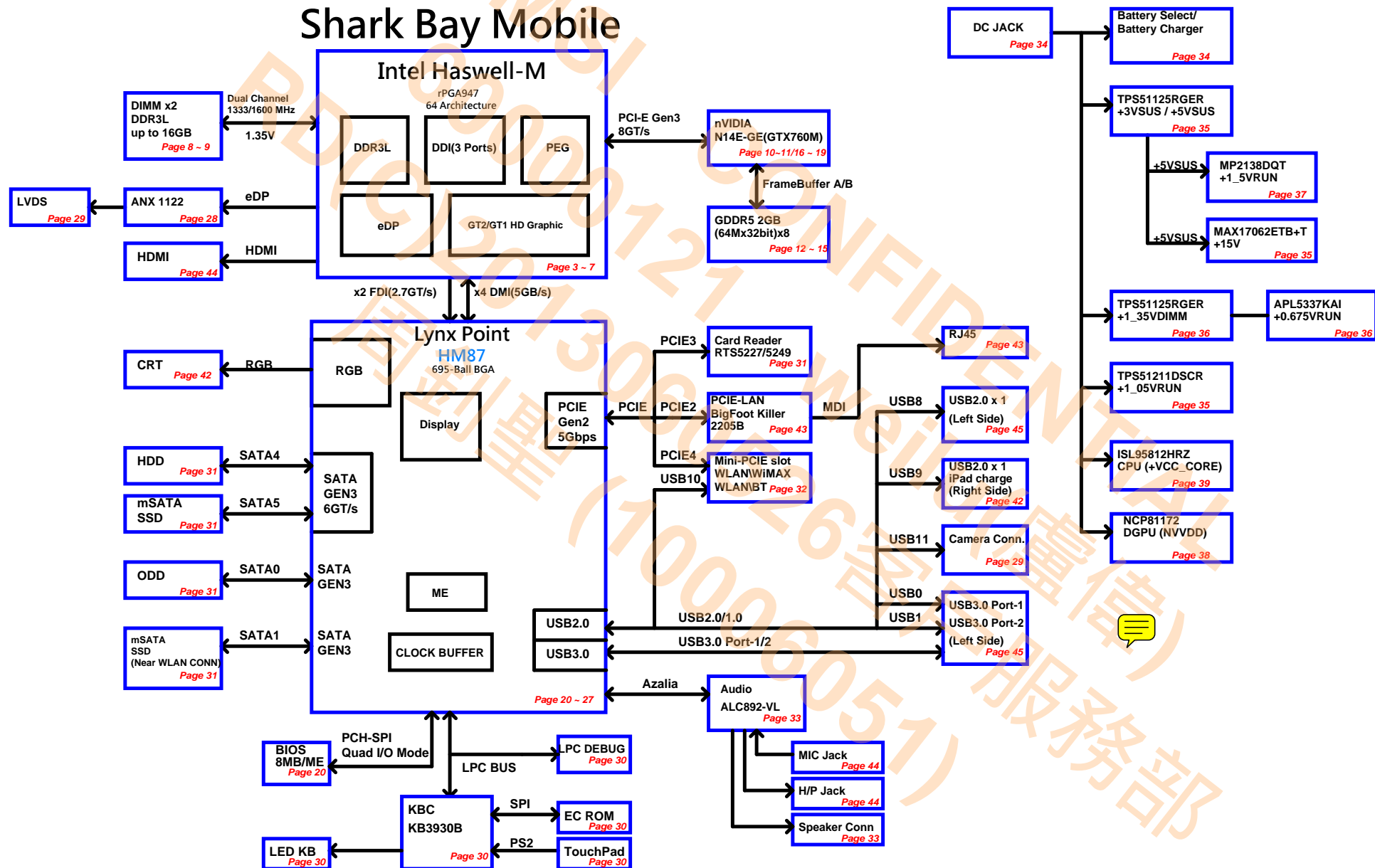


# MS-16GC ver:1.0

## Shark Bay Mobile



# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

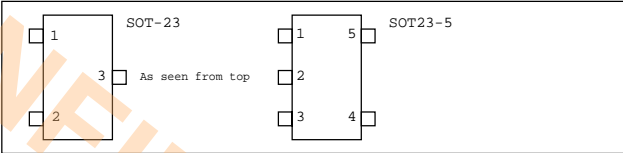
## Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
+5VALW	5.0V always on power rail	PWR_SRC
+3VALW	3.3V always on power rail	PWR_SRC
+5VSUS	5.0V power rail	SUS_ON
+3VSUS	3.3V power rail	SUS_ON
+1_35VDIMM	1.35V DDR3L power rail (off in S4-S5)	PM_SLP_S4#
+0_675VRUN	0.675V DDR3L Termination voltage (off in S3-S5)	PM_SLP_S3#
+5VRUN	5.0V switched power rail (off in S3-S5)	PM_SLP_S3#
+3VRUN	3.3V switched power rail (off in S3-S5 / M0)	PM_SLP_S3#
+1_5VRUN	1.5V switched power rail (off in S3-S5)	PM_SLP_S3#
+VCC_CORE	1.2V Core Voltage for Processor	VR_ON
+1_05VRUN	1.05V rail for Processor	PM_SLP_S3#
NVDD	0.6~1.2V(VBoot:0.9V)Core Voltage for nVIDIA N14E-GE DGPU	GPIO11_GPUVID
+3V3_NV	3.3V GPU I/O power rail (off in Optimus OFF)	DGPU_PWR_EN#
FBVDDQ	1.35V FB / GDDR5 power rail (off in Optimus OFF)	GPU_PWRGD
PEX_VDD	1.05V PLL power rail (off in Optimus OFF)	GPU_PWRGD

## Net Naming Conventions

<b>Suffix</b>
# = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

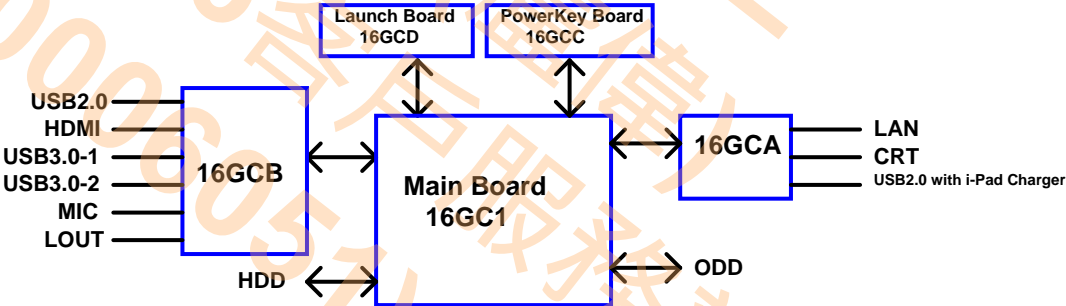
## PCB Footprints



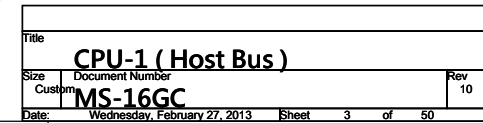
## POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+V*ALW	+*VSUS	+*VRUN	Clocks
S0( Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3( Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4( Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V\*SUS will always keep high



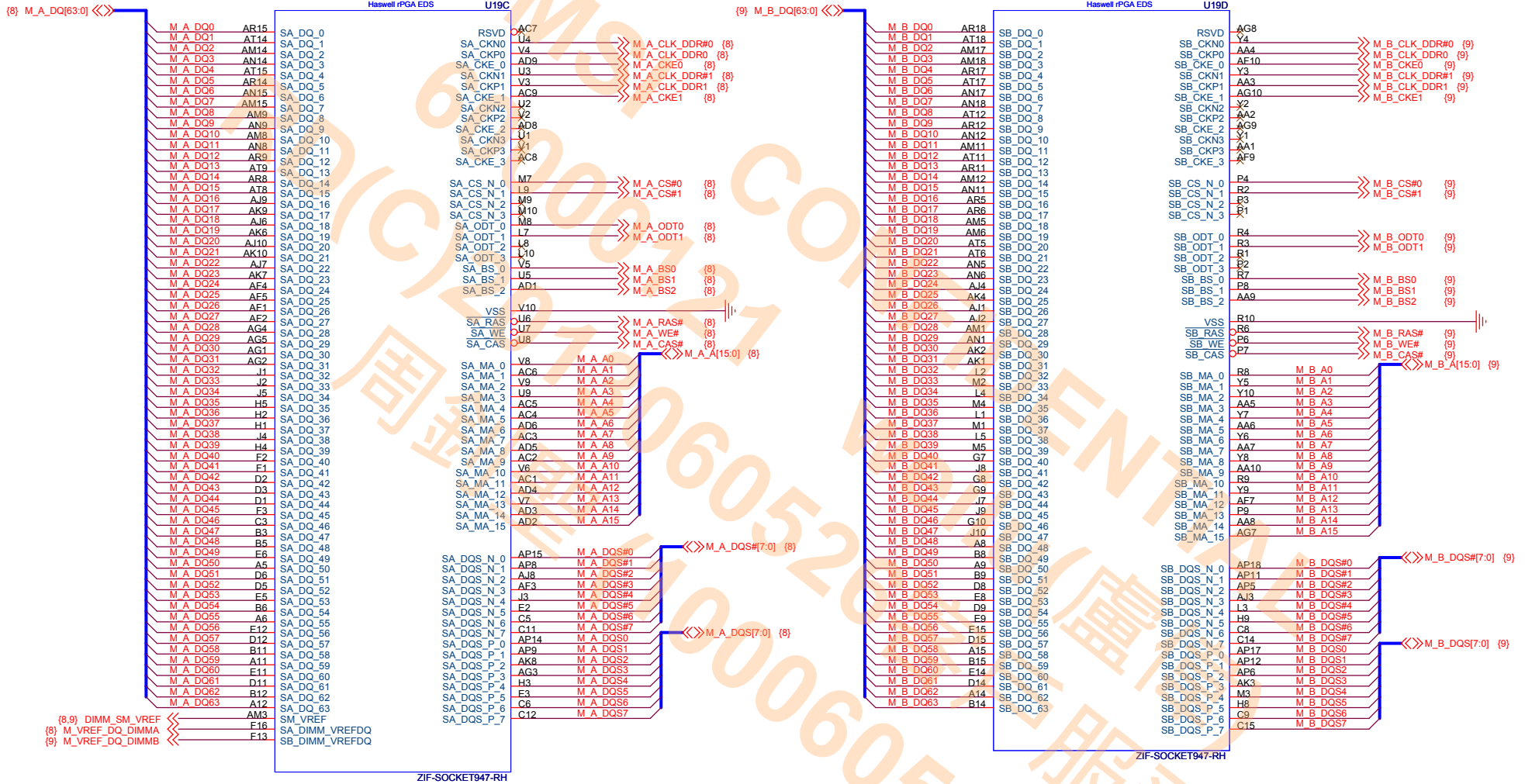
Haswell ( CLK,MISC,JTAG )



# Haswell (DDR3L)

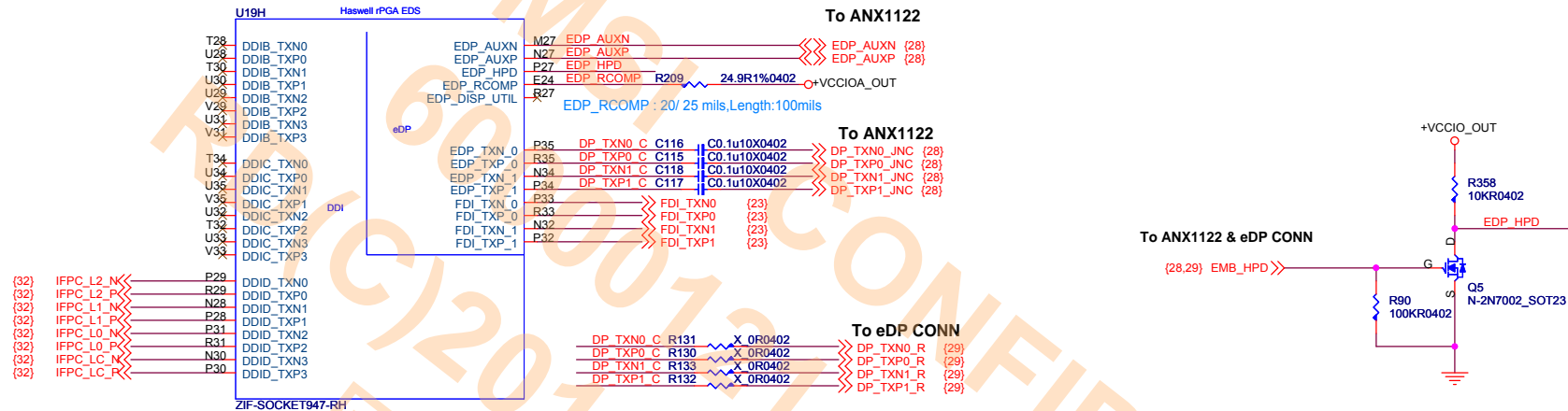
## SODIMM#A

## SODIMM#B

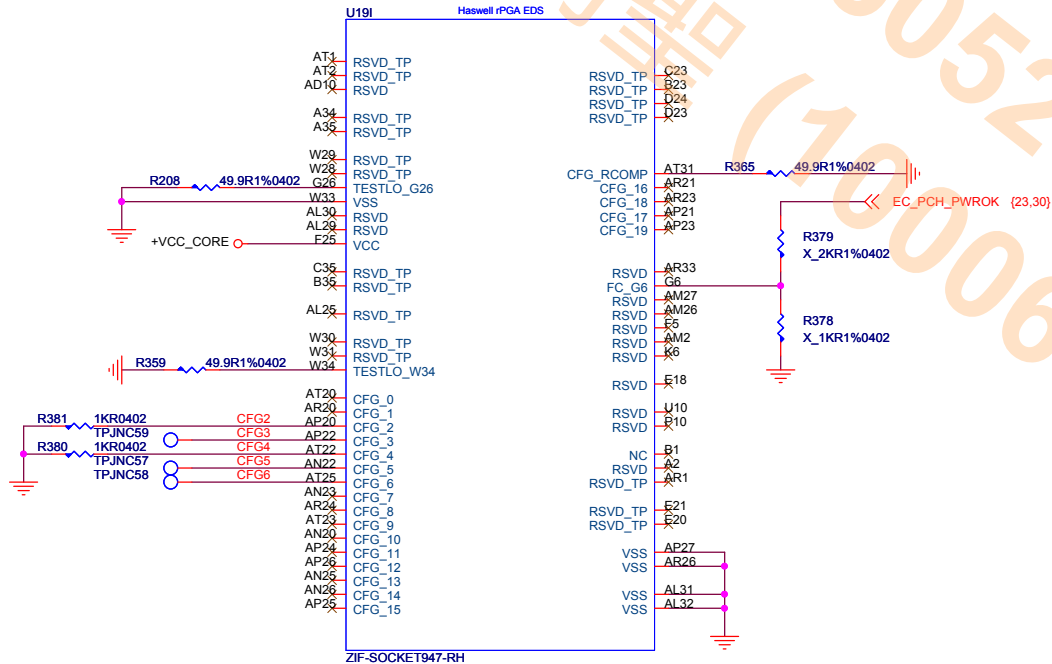


Title	
CPU-2 (DDR3L)	
Size	Document Number
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## Haswell ( Display )



## Haswell ( Reserved )



PCI Express* Static x16 Lane Numbering Reversal	
CFG2	1 = Normal operation 0 = Lane numbers reversed.

MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

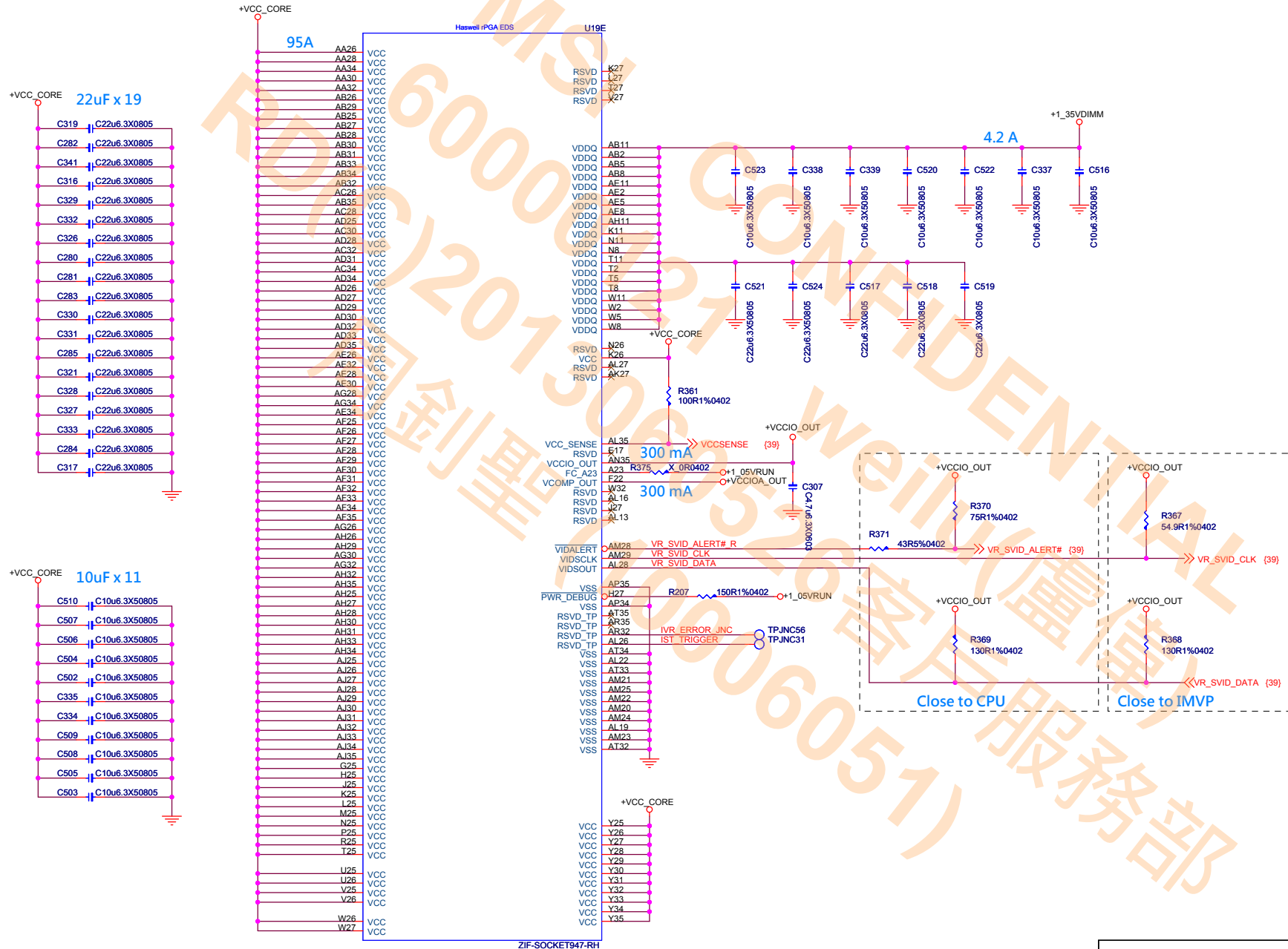
eDP enable	
CFG4	1 = Disabled 0 = Enabled

PCI Express* Bifurcation	
CFG[5,6]	00 = 1 x8, 2 x4 PCI Express 01 = reserved 10 = 2 x8 PCI Express 11 = 1 x16 PCI Express

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train Immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Title		
CPU-3 ( Display/Reserved )		
Size	Document Number	Rev
Custom	MS-16GC	10
Date: Wednesday, February 27, 2013		Sheet 5 of 50

# Haswell ( POWER )



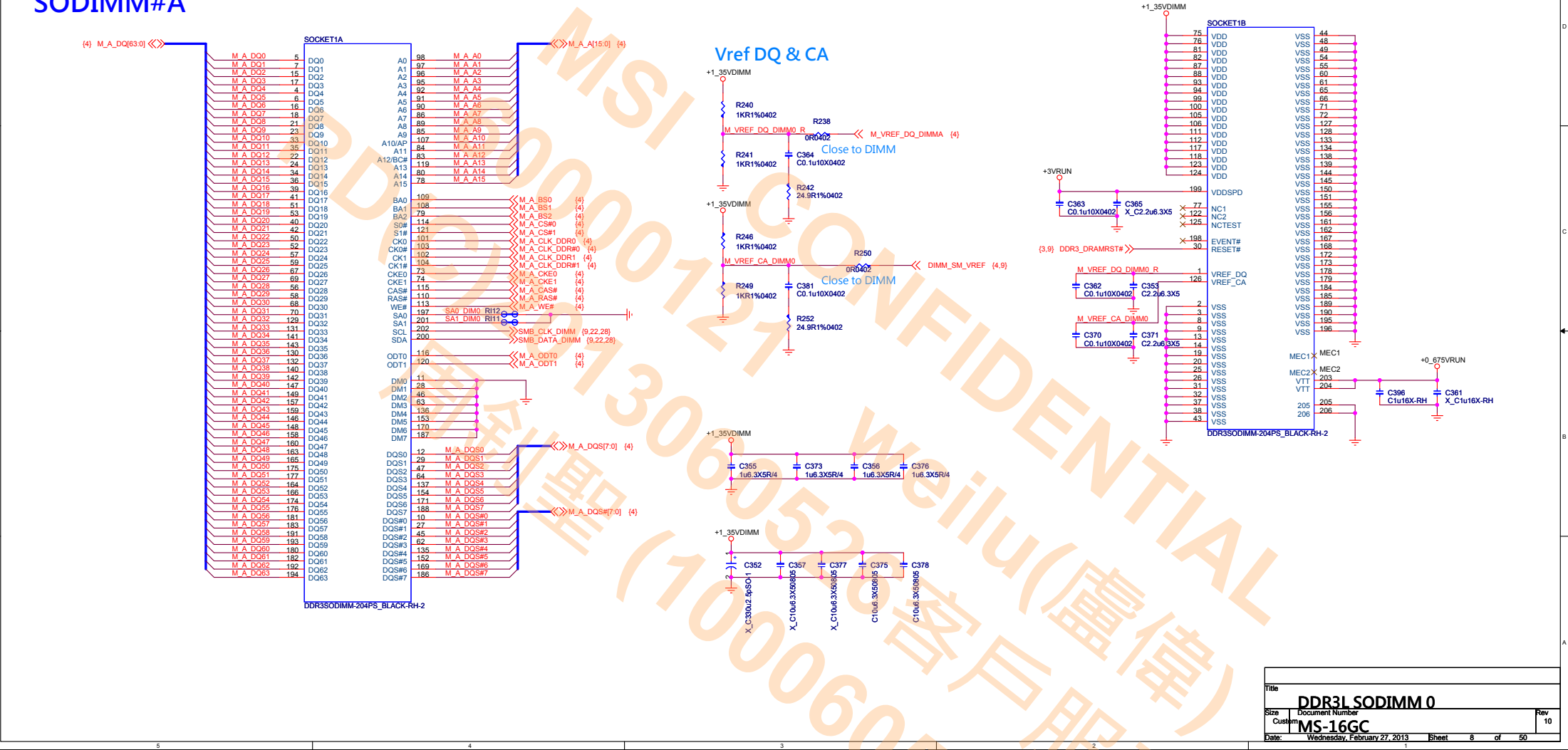
Title		
CPU-4 ( Power )		
Size	Document Number	Rev
Custom	MS-16GC	10
Date:	Wednesday, February 27, 2013	Sheet 6 of 50



Haswell ( GND )



SODIMM#A

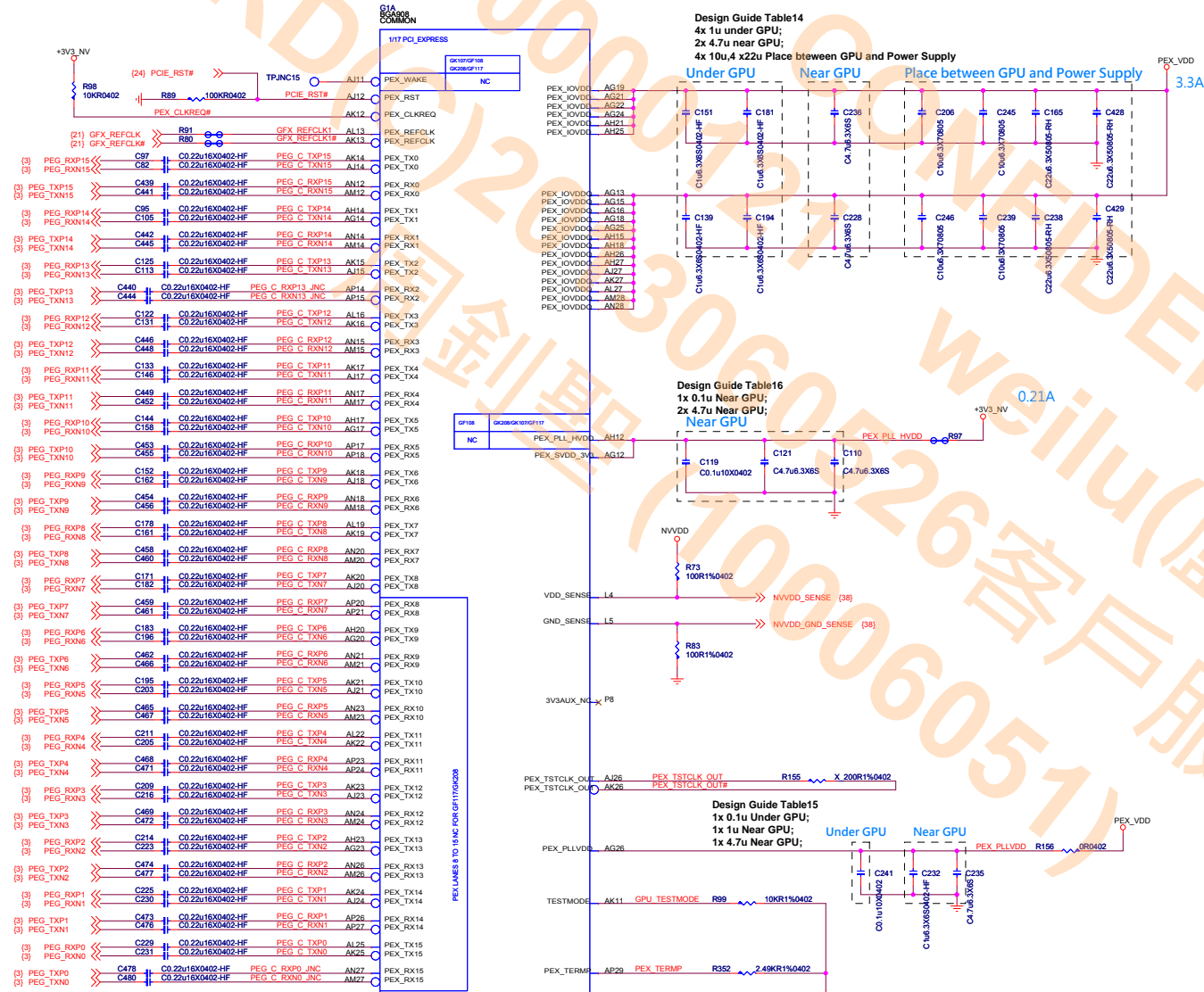
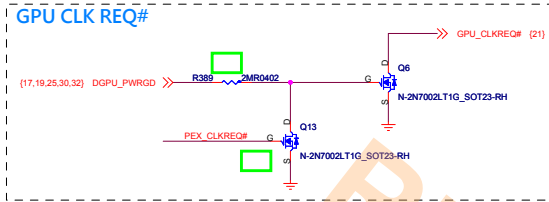


Title		
DDR3L SODIMM 0		
Size	Document Number	Rev
Customer	MS-16GC	10
Date:	Wednesday, February 27, 2013	Sheet 8 of 50

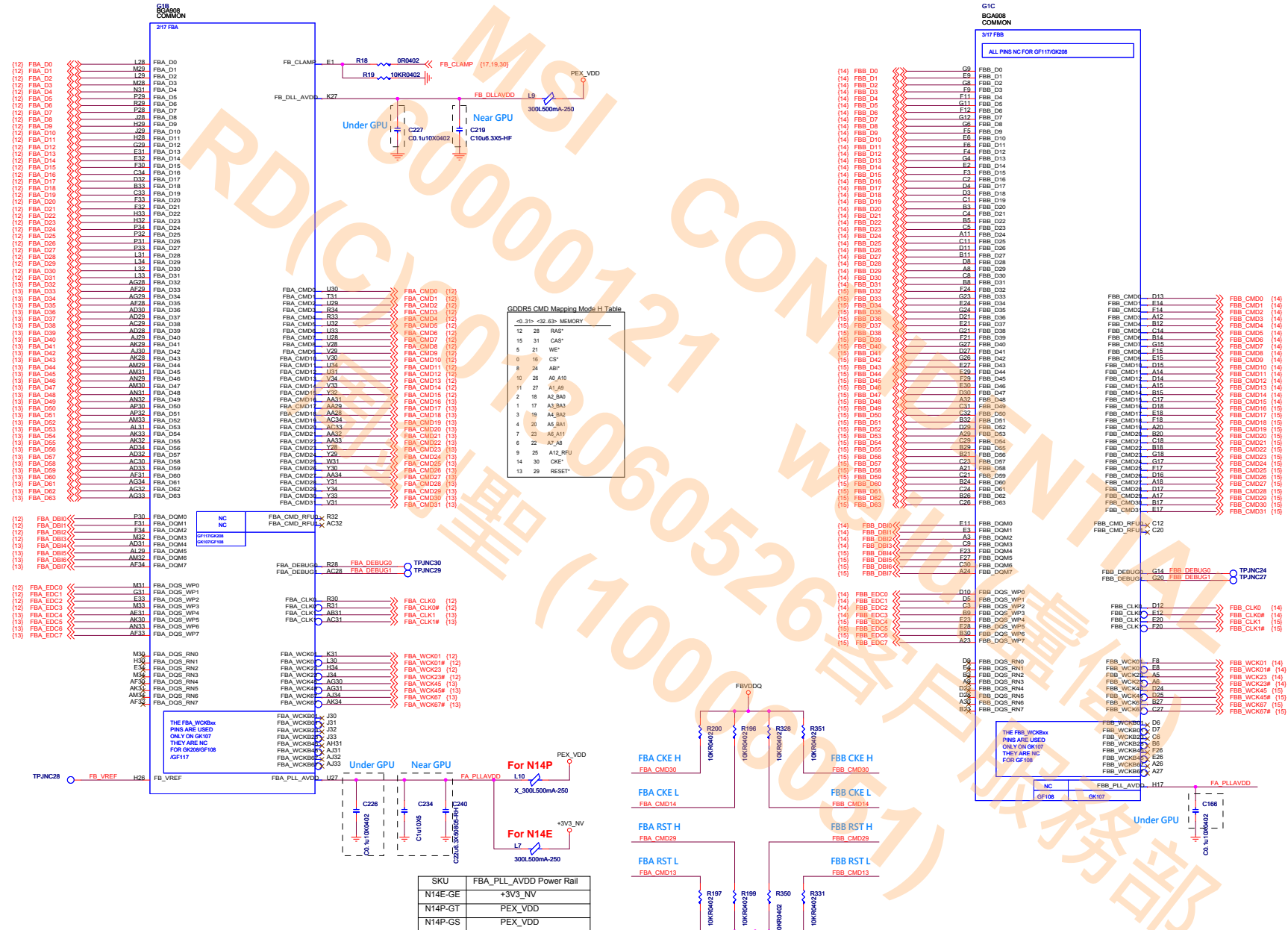




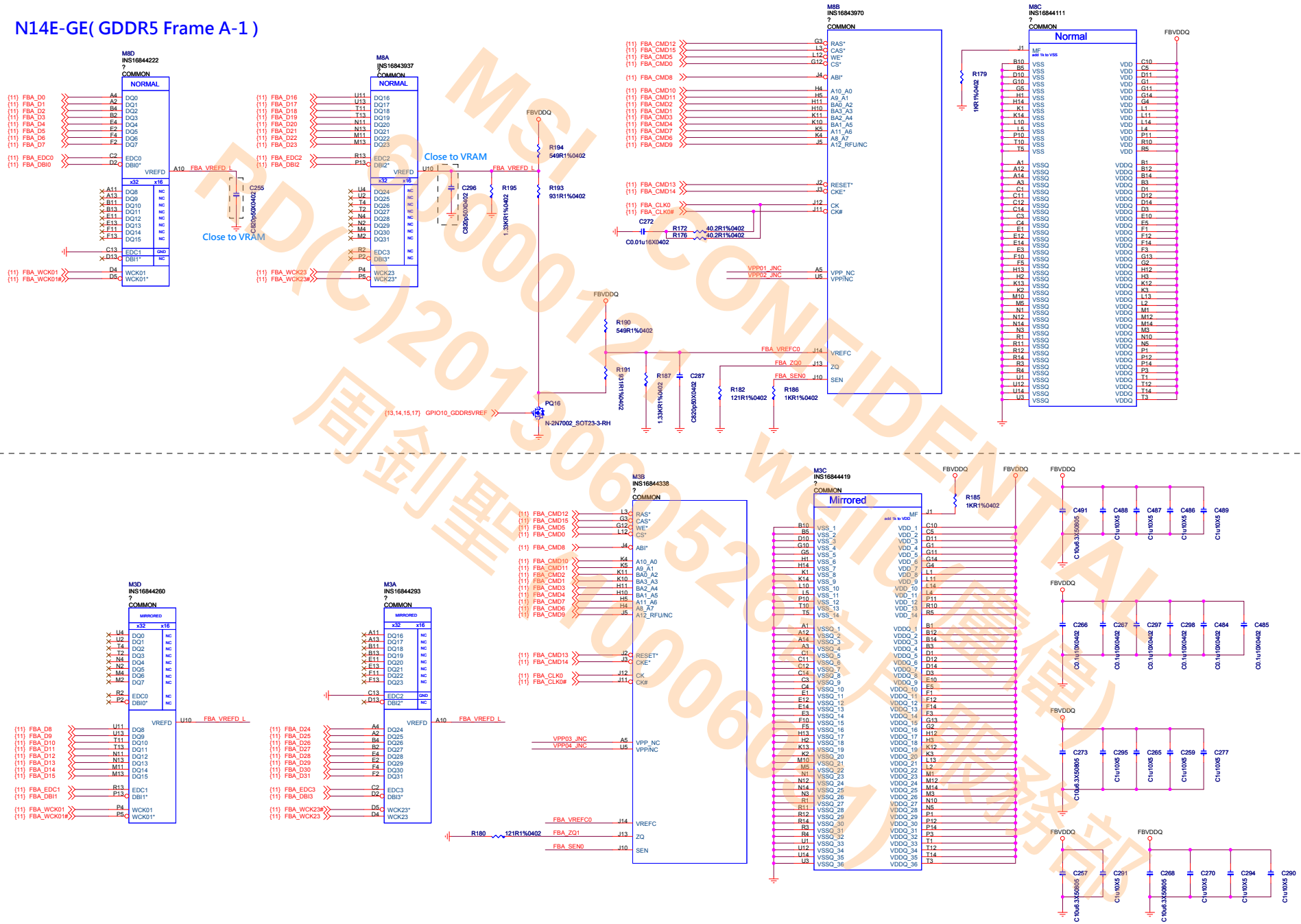
N14E-GE( PCI-Express Gen3 x16 Interface)



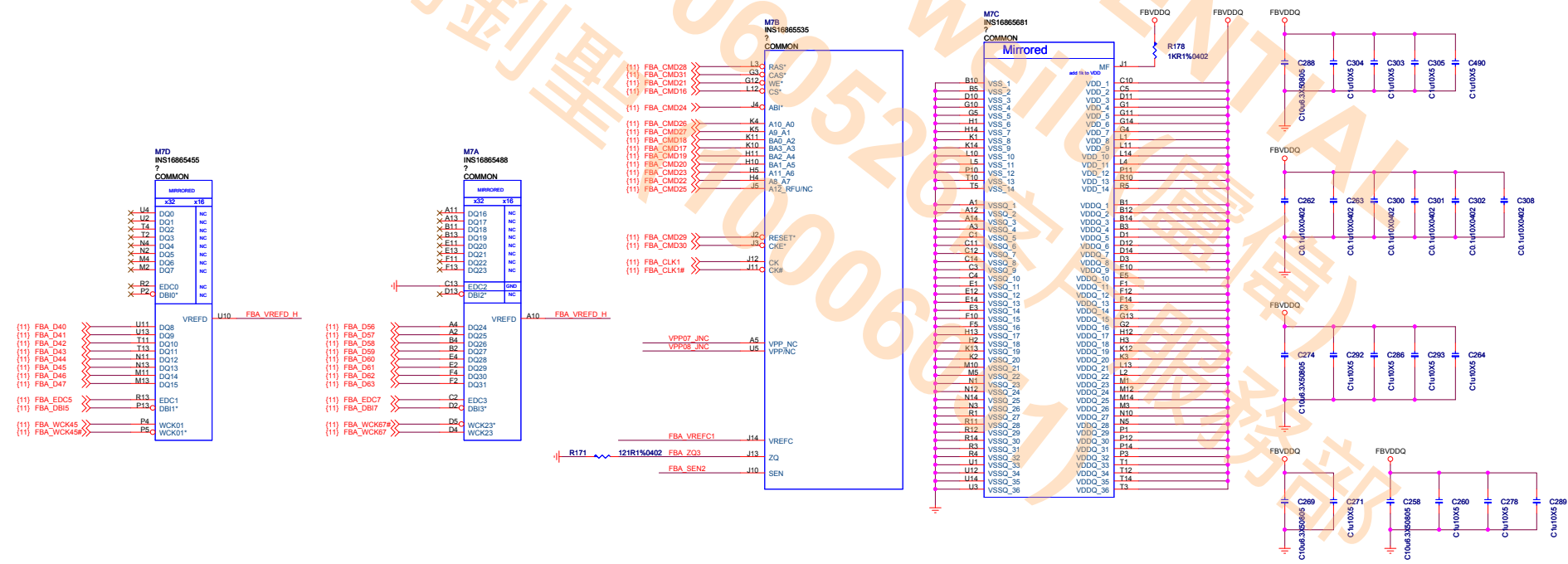
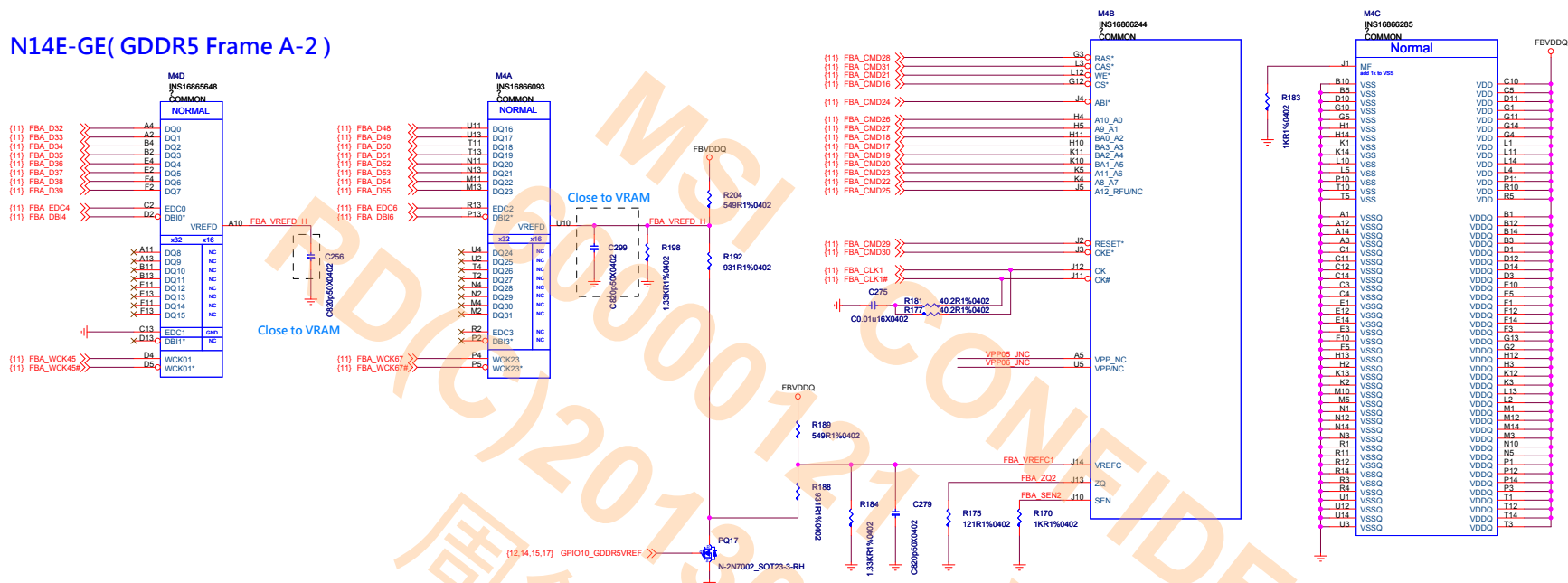
## N14E-GE( Frame Buffer Interface )



# N14E-GE( GDDR5 Frame A-1 )

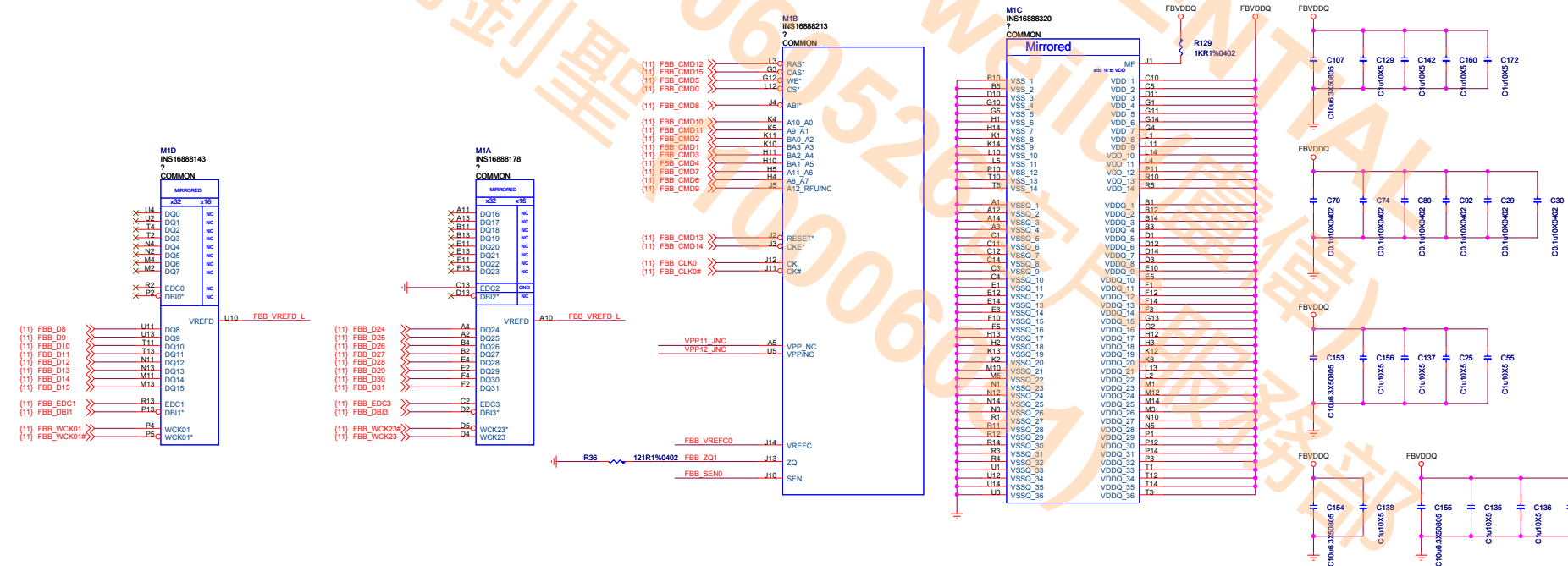
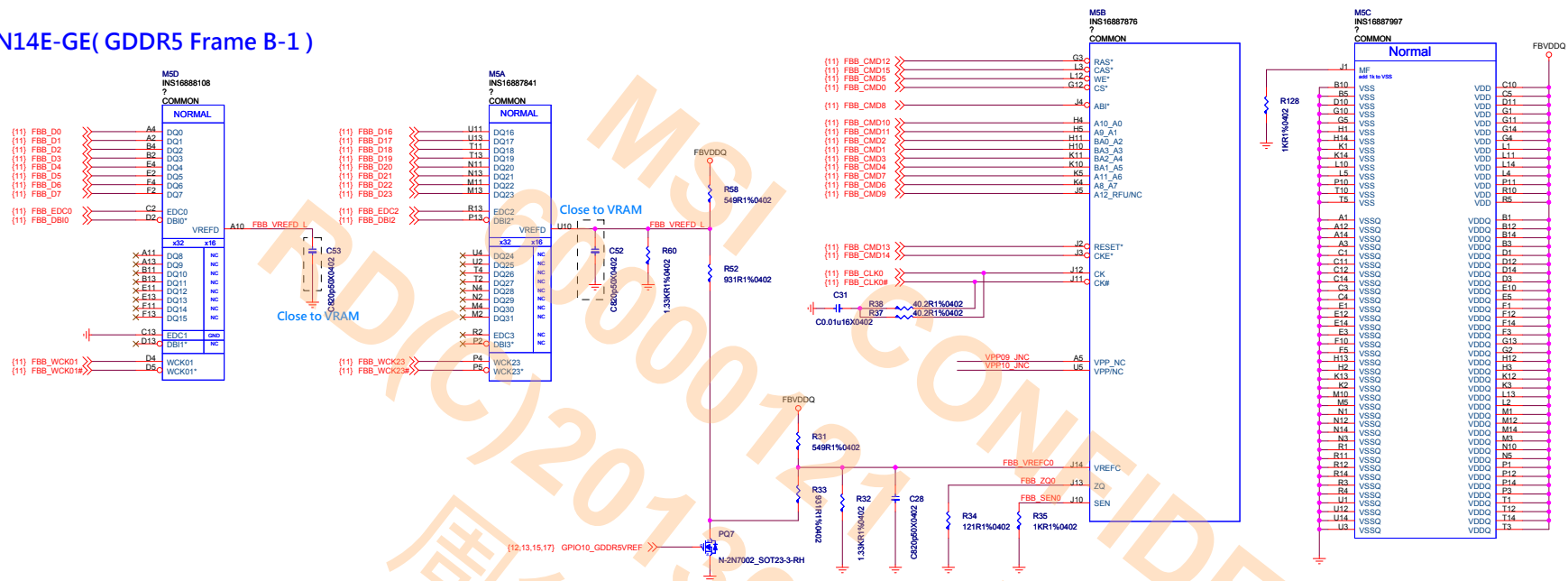


N14E-GE( GDDR5 Frame A-2 )



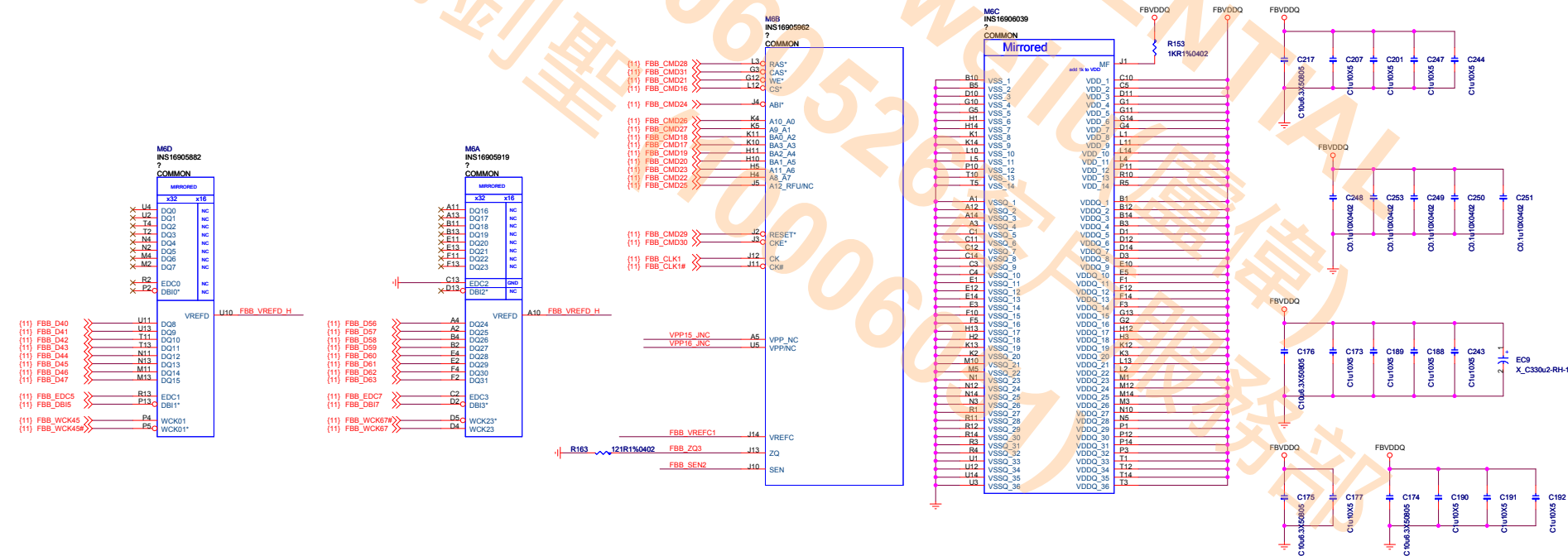
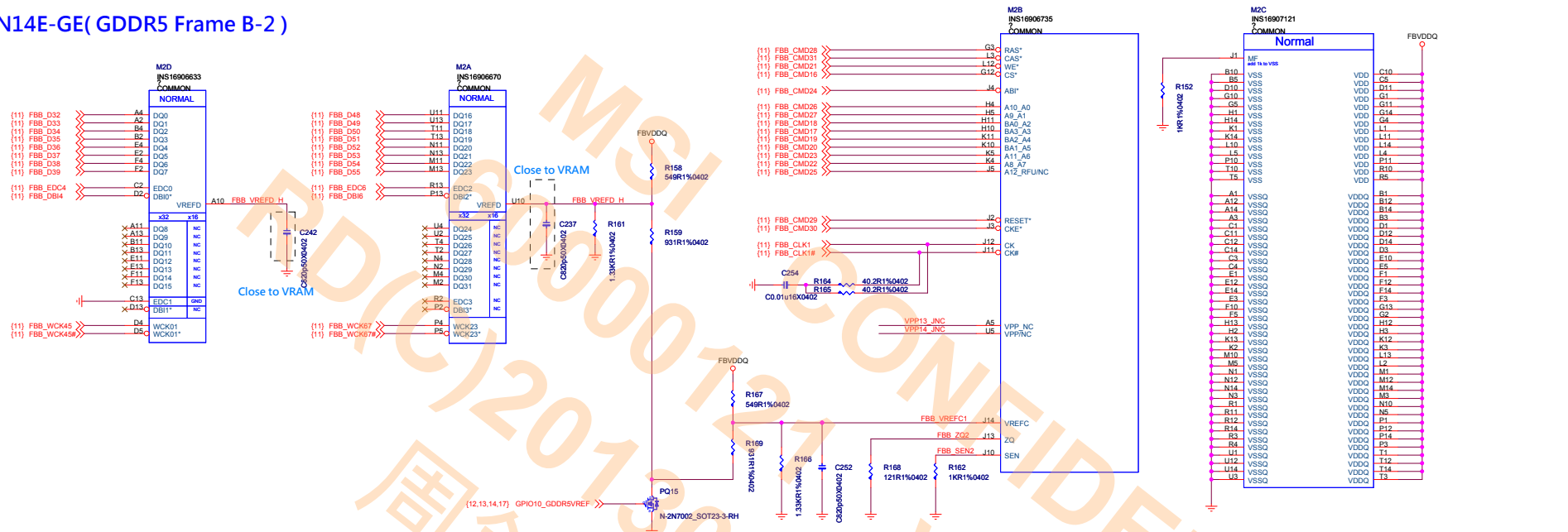


N14E-GE( GDDR5 Frame B-1 )



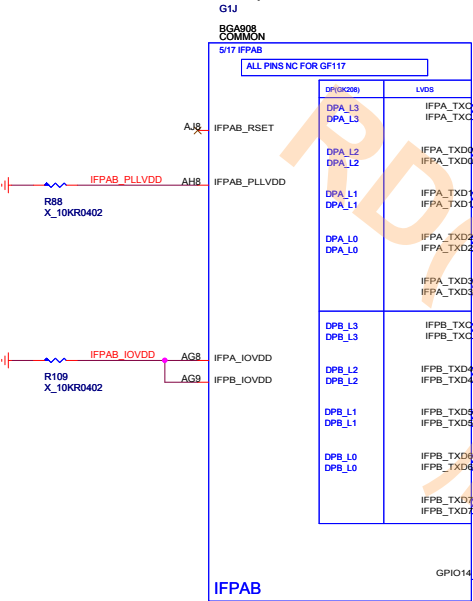


N14E-GE( GDDR5 Frame B-2 )

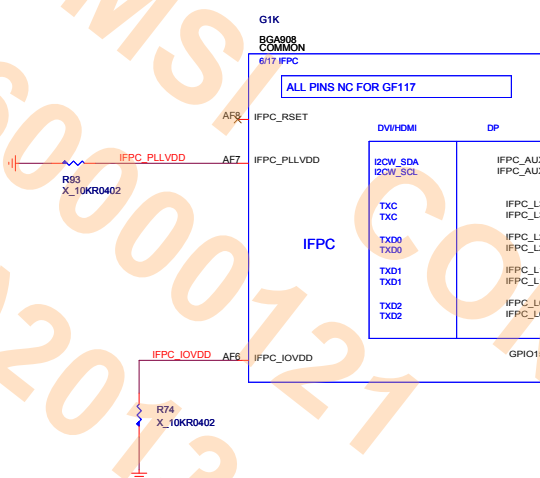


N14E-GE( Display IF)

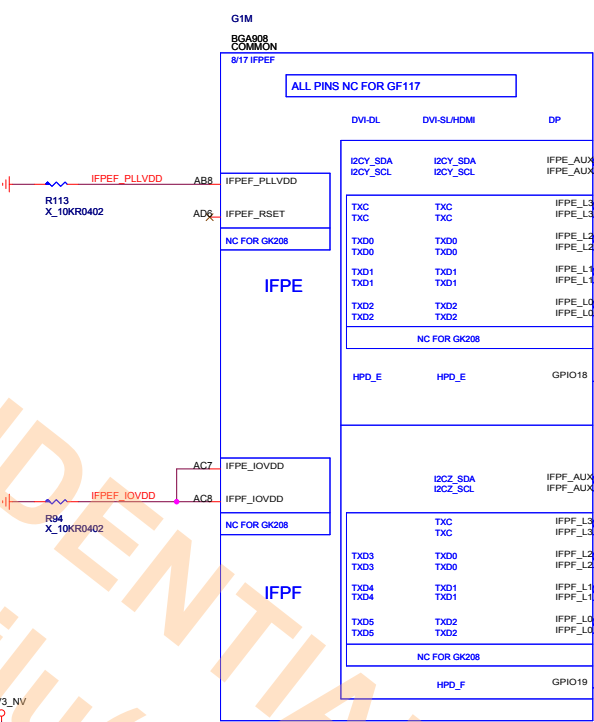
IFP A/B LVDSDual Link



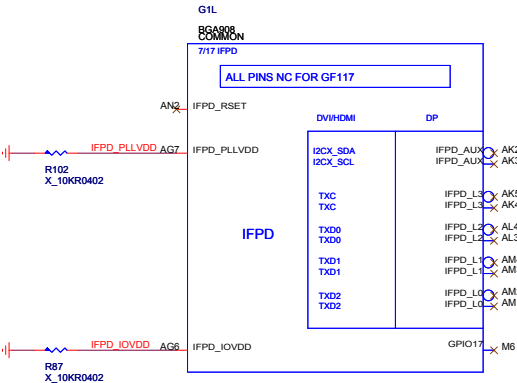
IFP C Native HDMI OR DP



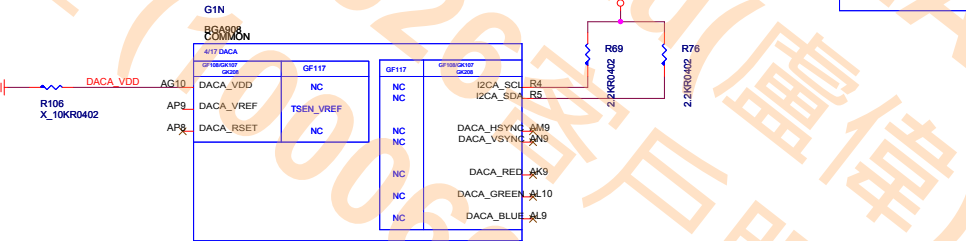
IFP E/F Dual Link TMDS DVI-I



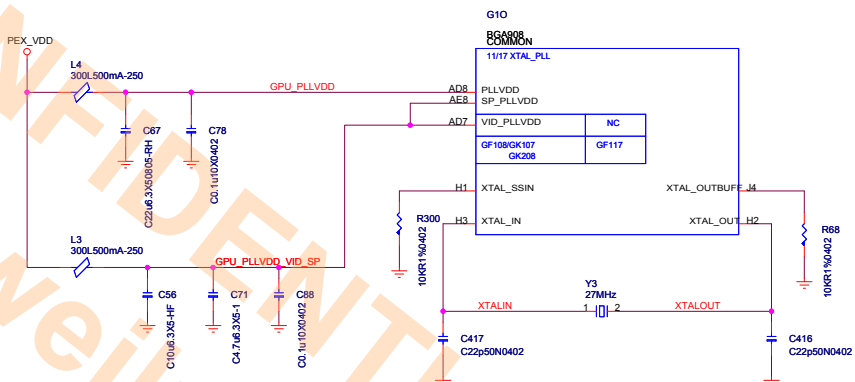
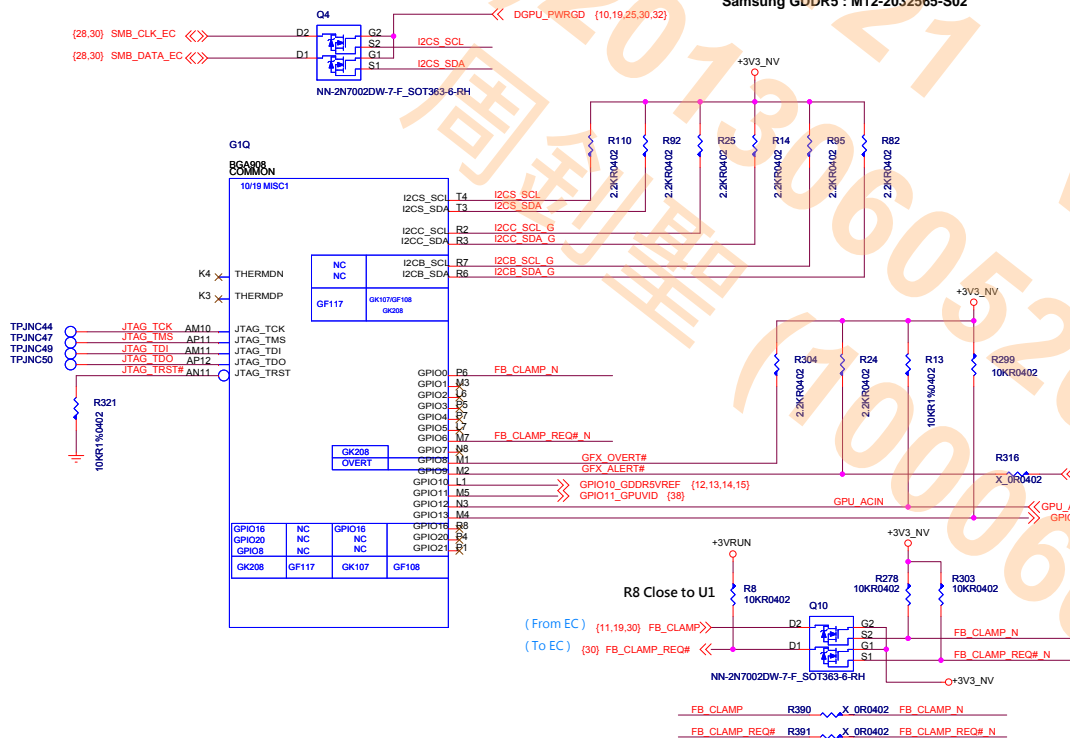
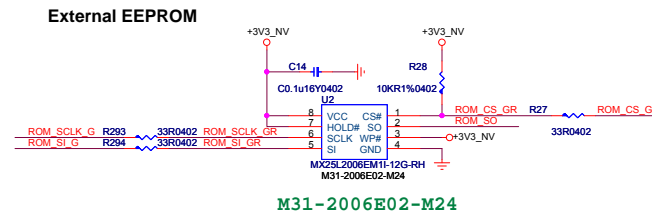
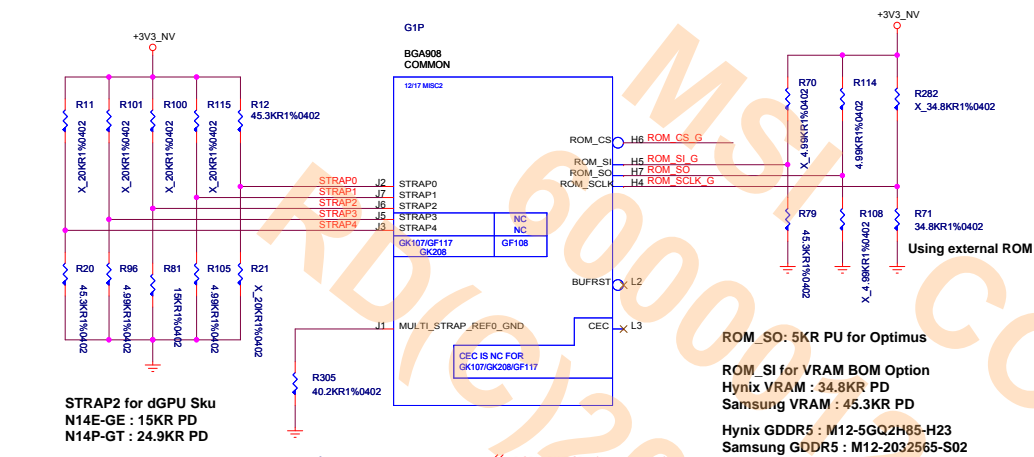
IFP D Dual Mode DP



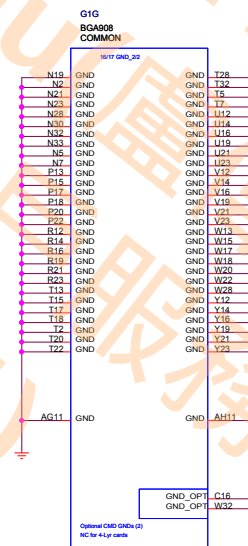
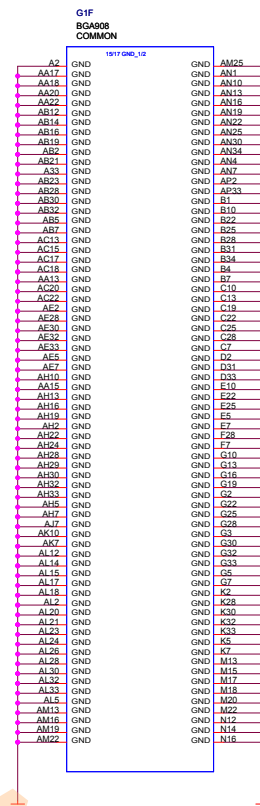
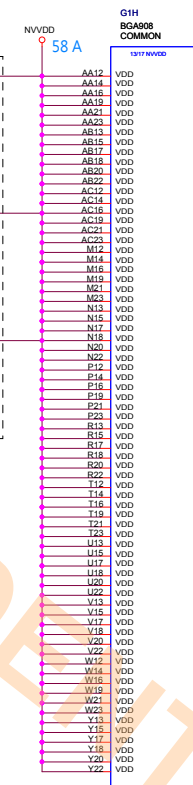
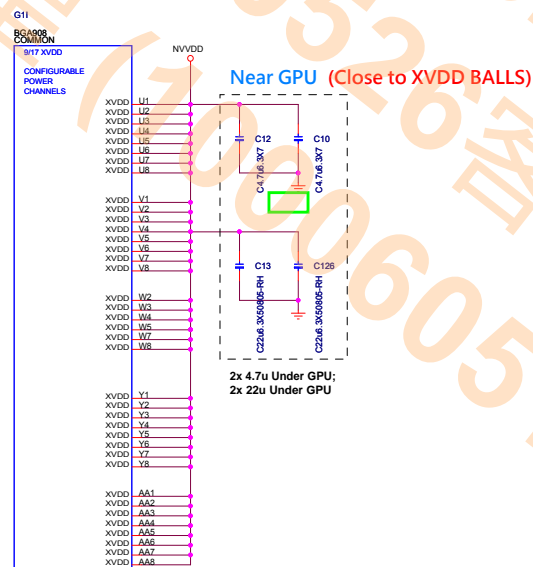
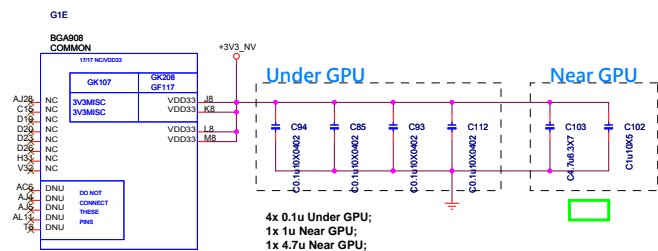
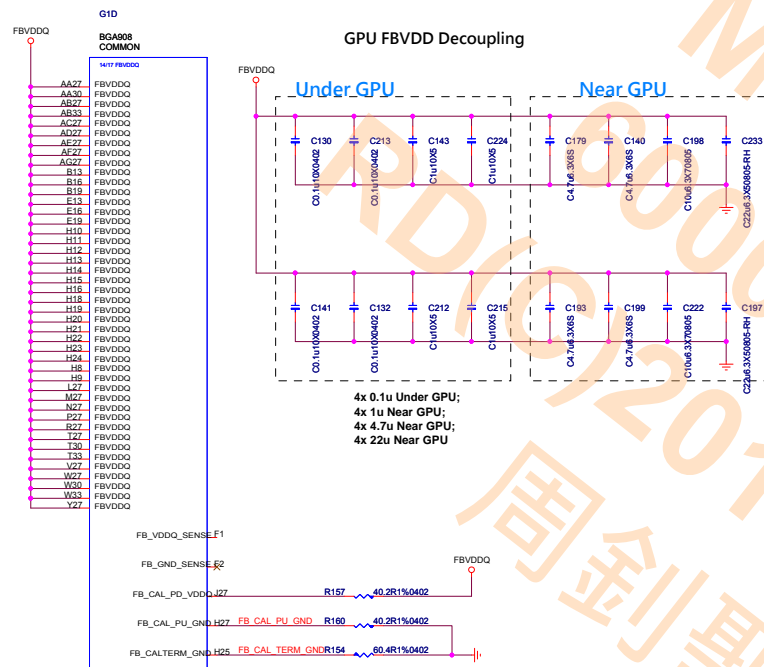
DAC A VGA



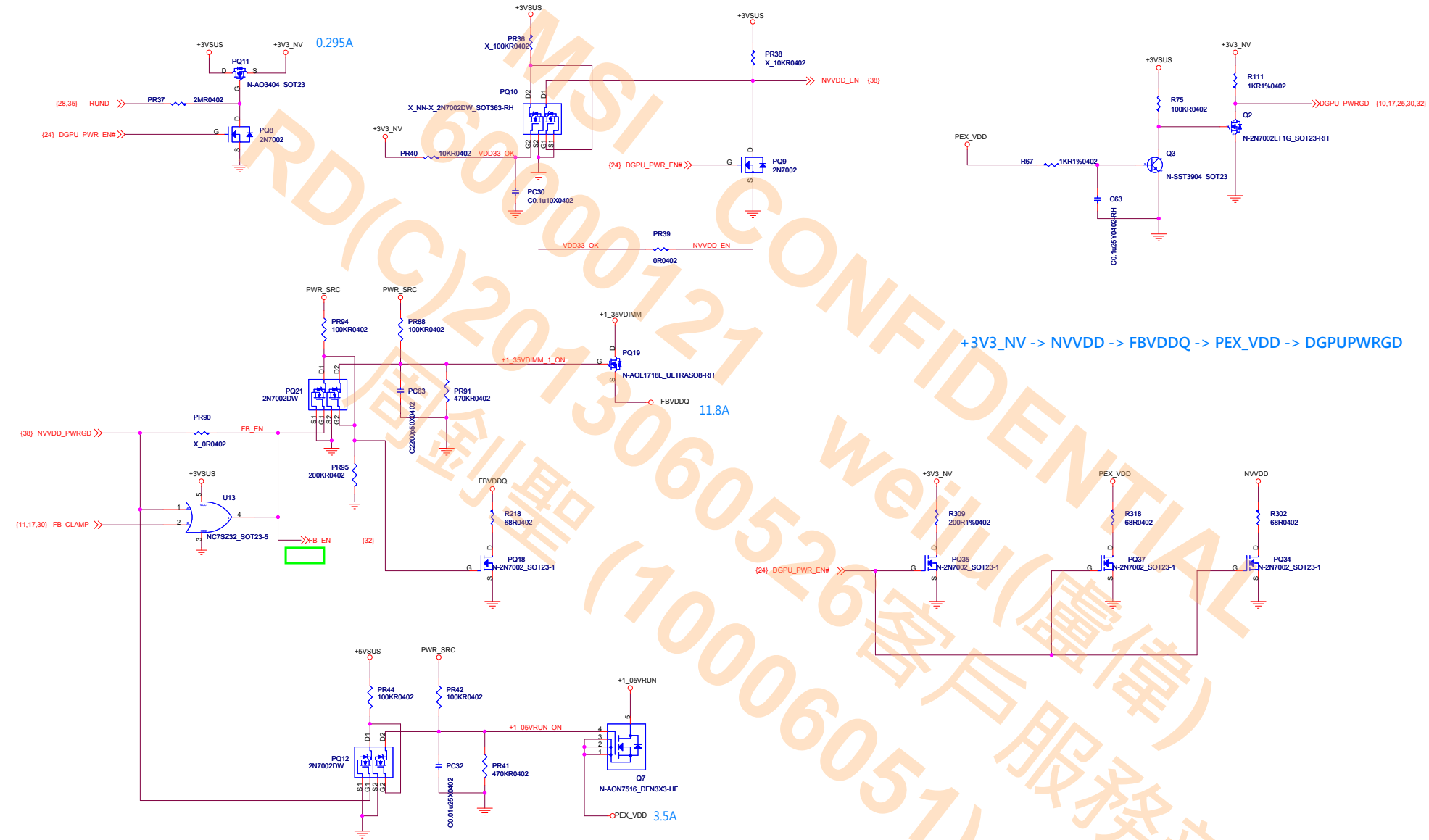
## N14E-GE( Thermal & GPIO )



Title				N14E-GE_Thermal & GPIO			
Size		Document Number				Rev	
Custom		MS-16GC				10	
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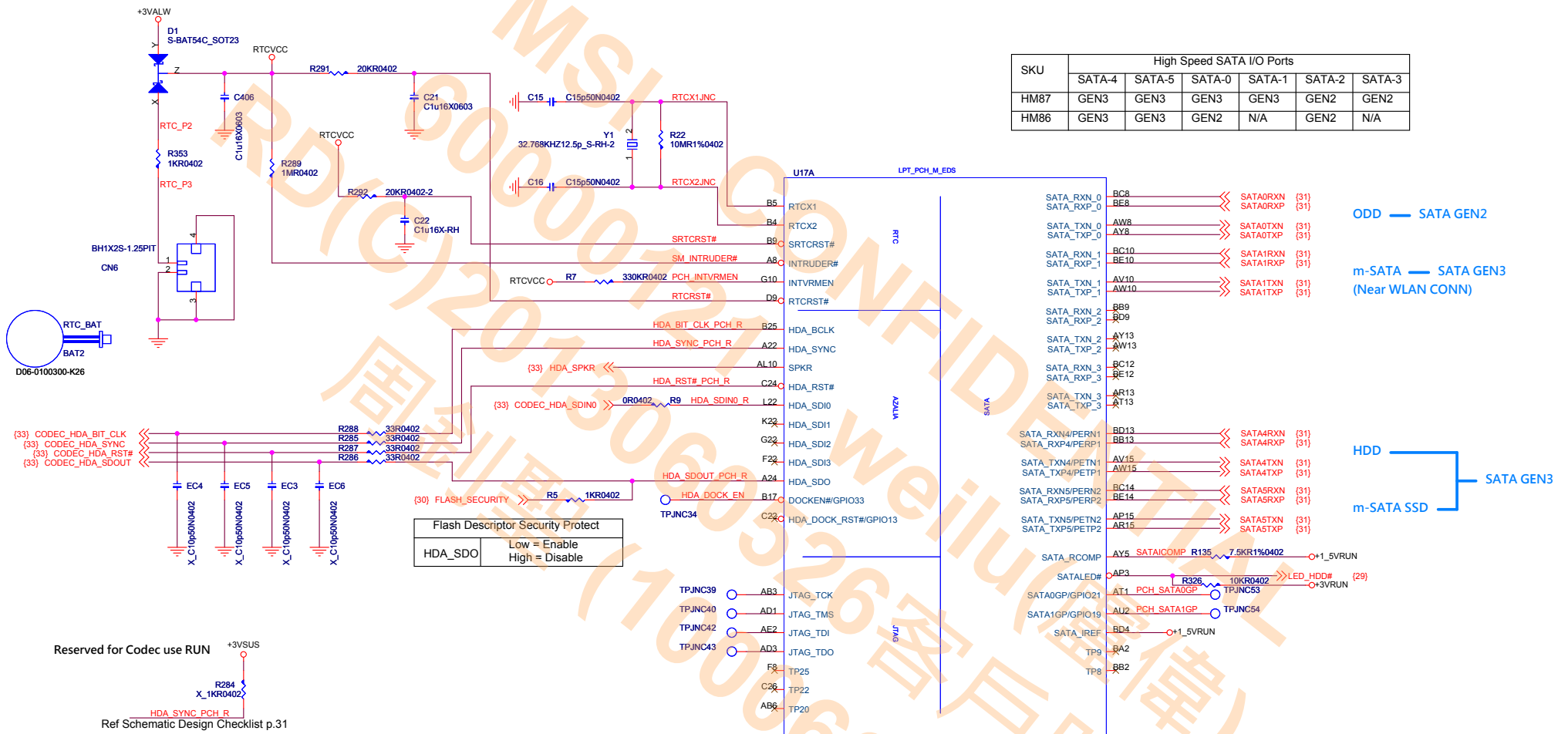


# N14E-GE( Power Control )



File			N14E-GE Power Control
Size	Document Number	Rev	
Custom	MS-16GC	10	
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## Lynx Point ( HDA,JTAG,SATA )



SKU	High Speed SATA I/O Ports					
	SATA-4	SATA-5	SATA-0	SATA-1	SATA-2	SATA-3
HM87	GEN3	GEN3	GEN3	GEN3	GEN2	GEN2
HM86	GEN3	GEN3	GEN2	N/A	GEN2	N/A

ODD — SATA GEN2

m-SATA — SATA GEN3  
(Near WLAN CONN)

```

graph LR
    HDD --- SATA_GEN3[SATA GEN3]
    m_SATA_SSD[m-SATA SSD] --- SATA_GEN3

```

Flash Descriptor Security Protect	
HDA_SDO	Low = Enable High = Disable

Reserved for Codec use RUN +3VSUS

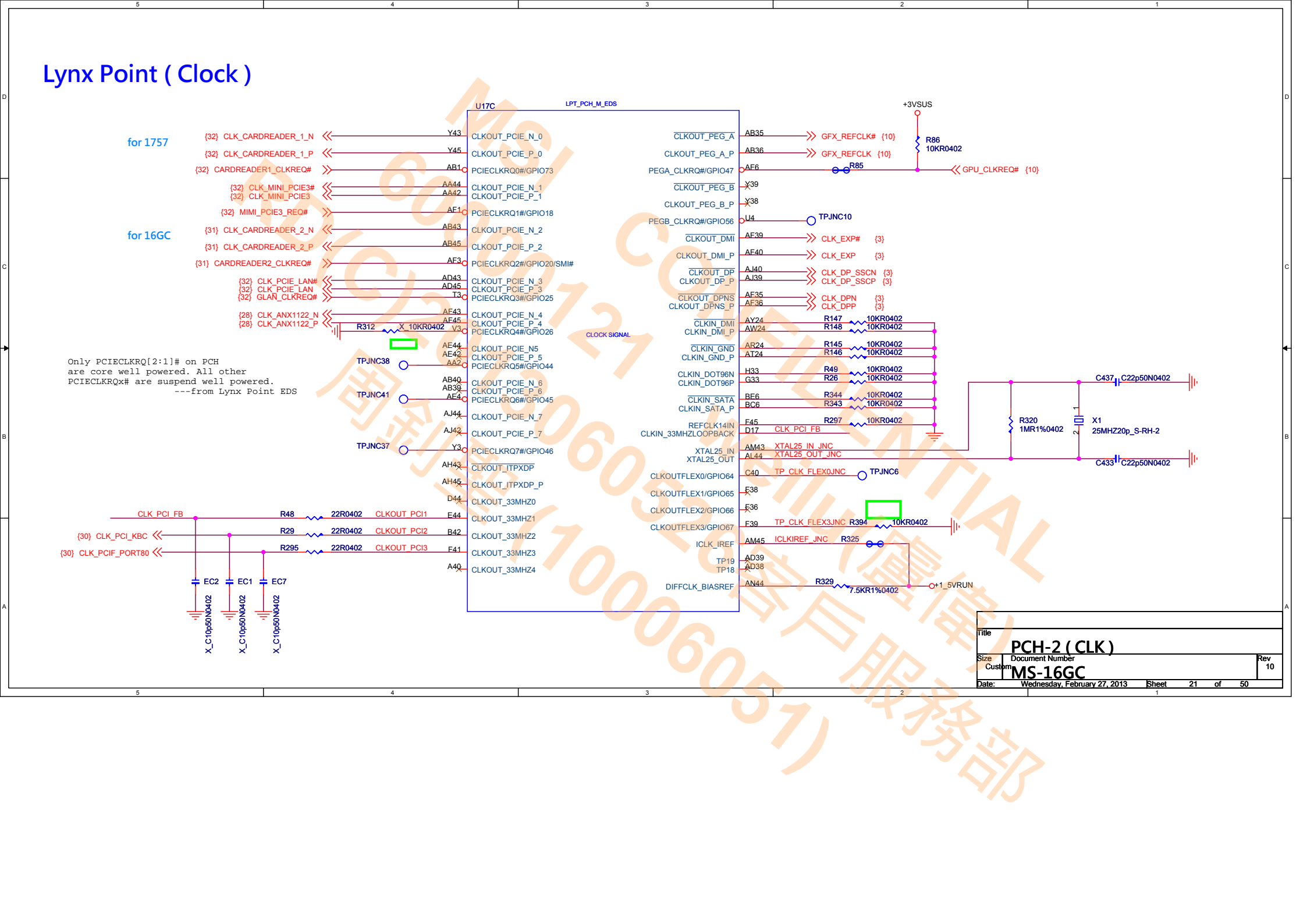
R284  
X\_1KR0402

HDA\_SYNC\_PCH\_R

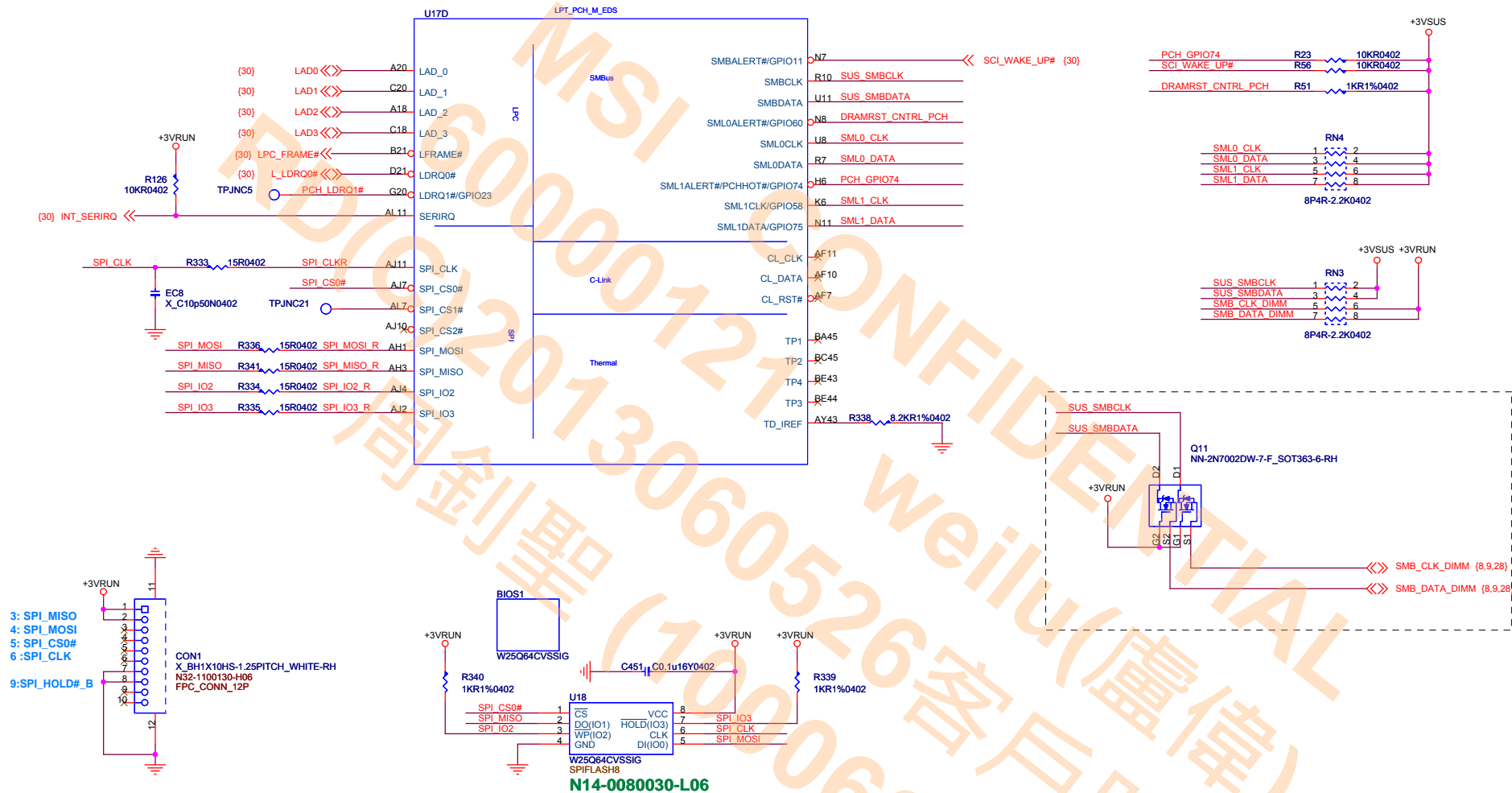
Ref Schematic Design Checklist p.31

Title			
PCH-1 ( HDA/JTAG/SATA )			
Size	Document Number	Rev	
Custom	MS-16GC	10	
Date:	Wednesday, February 27, 2013	Sheet	20 of 50

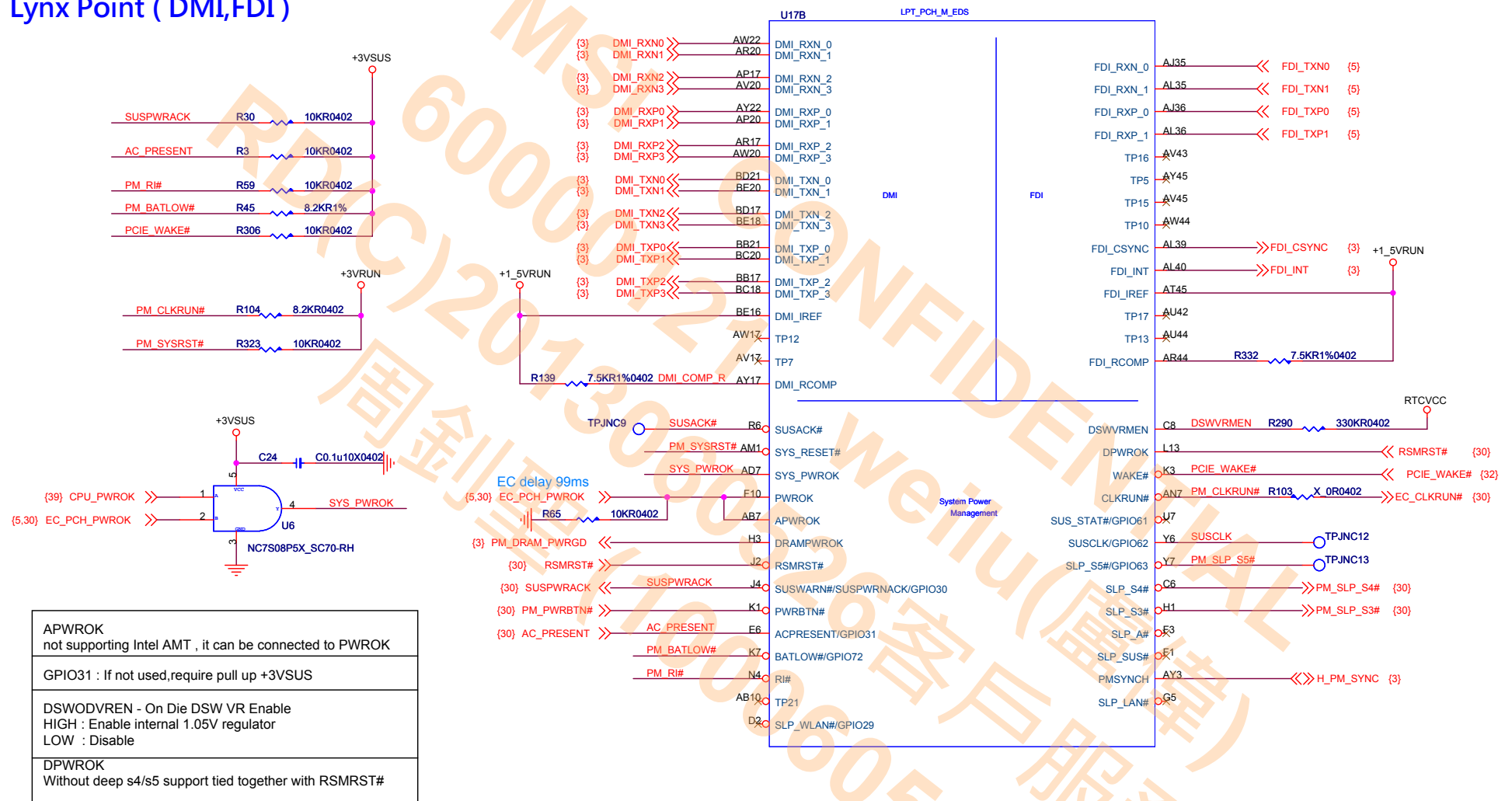


[illegible][illegible]

Lynx Point ( LPC,SMBUS )

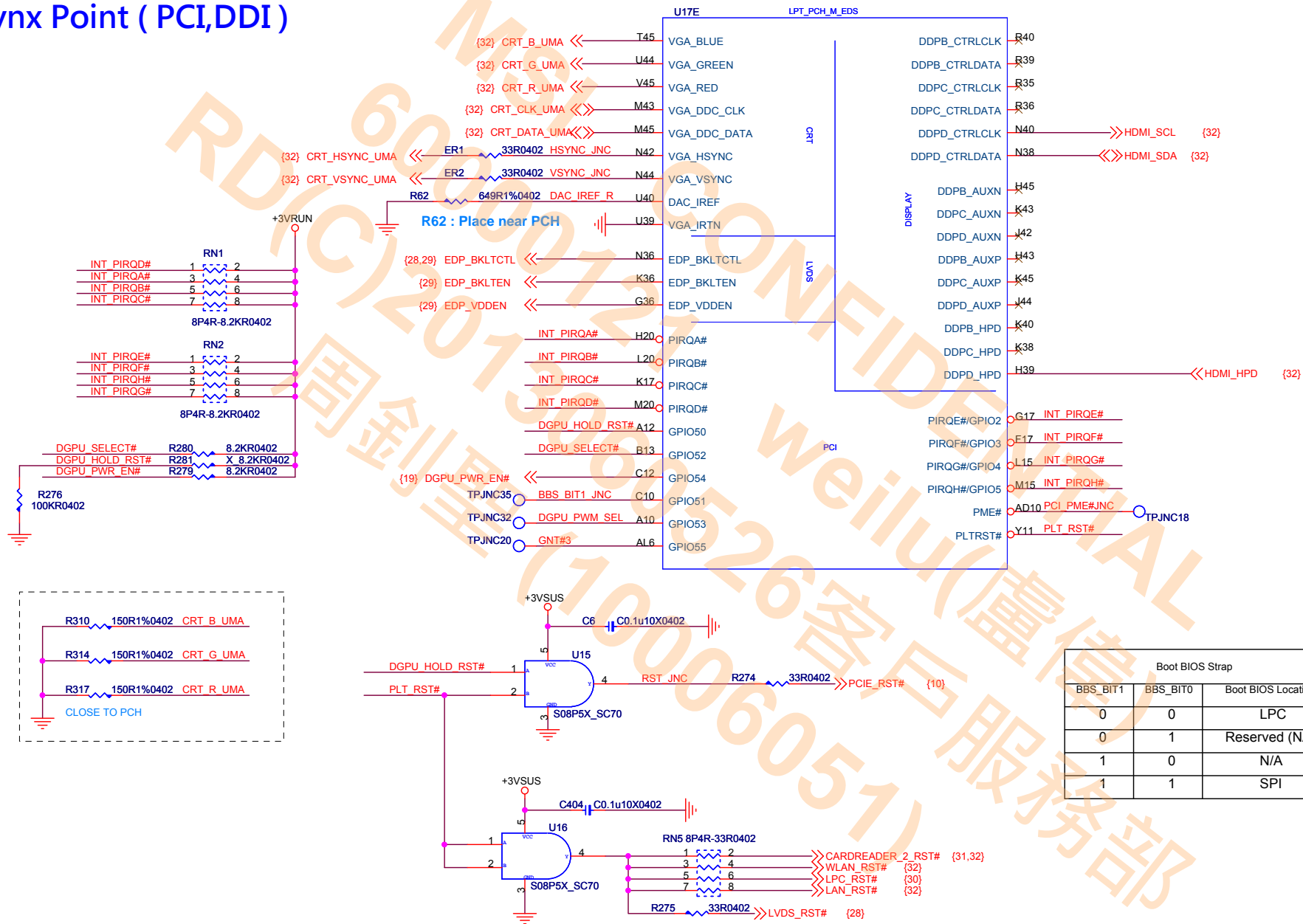


## Lynx Point ( DMI,FDI )



Title			PCH-4 ( DMI,FDI )
Size	Document Number	Rev	
Custom	MS-16GC	10	
Date:	Wednesday, February 27, 2013	Sheet	23 of 50

# Lynx Point ( PCI,DDI )

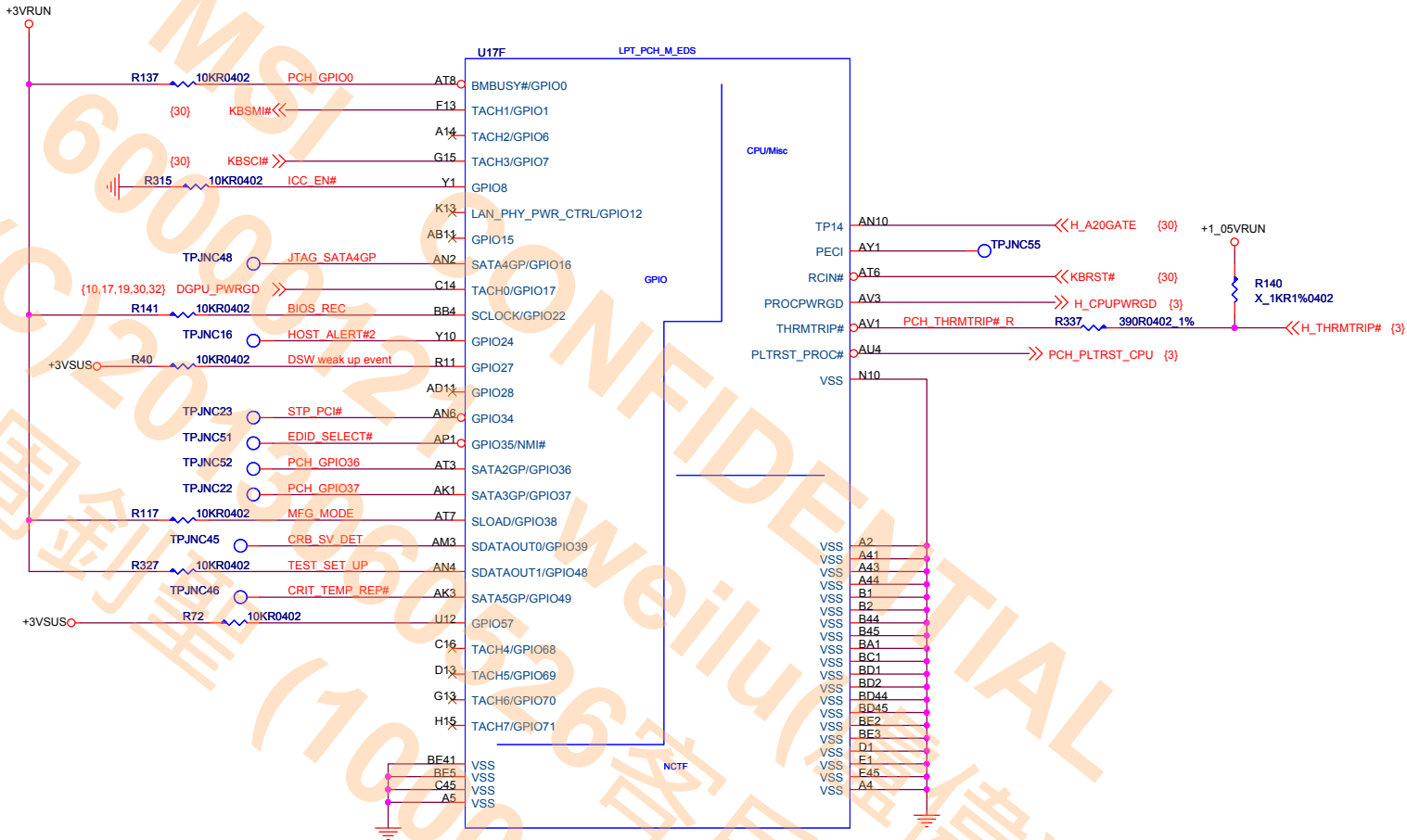


Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	N/A
1	1	SPI

# Lynx Point ( GPIO,MISC )

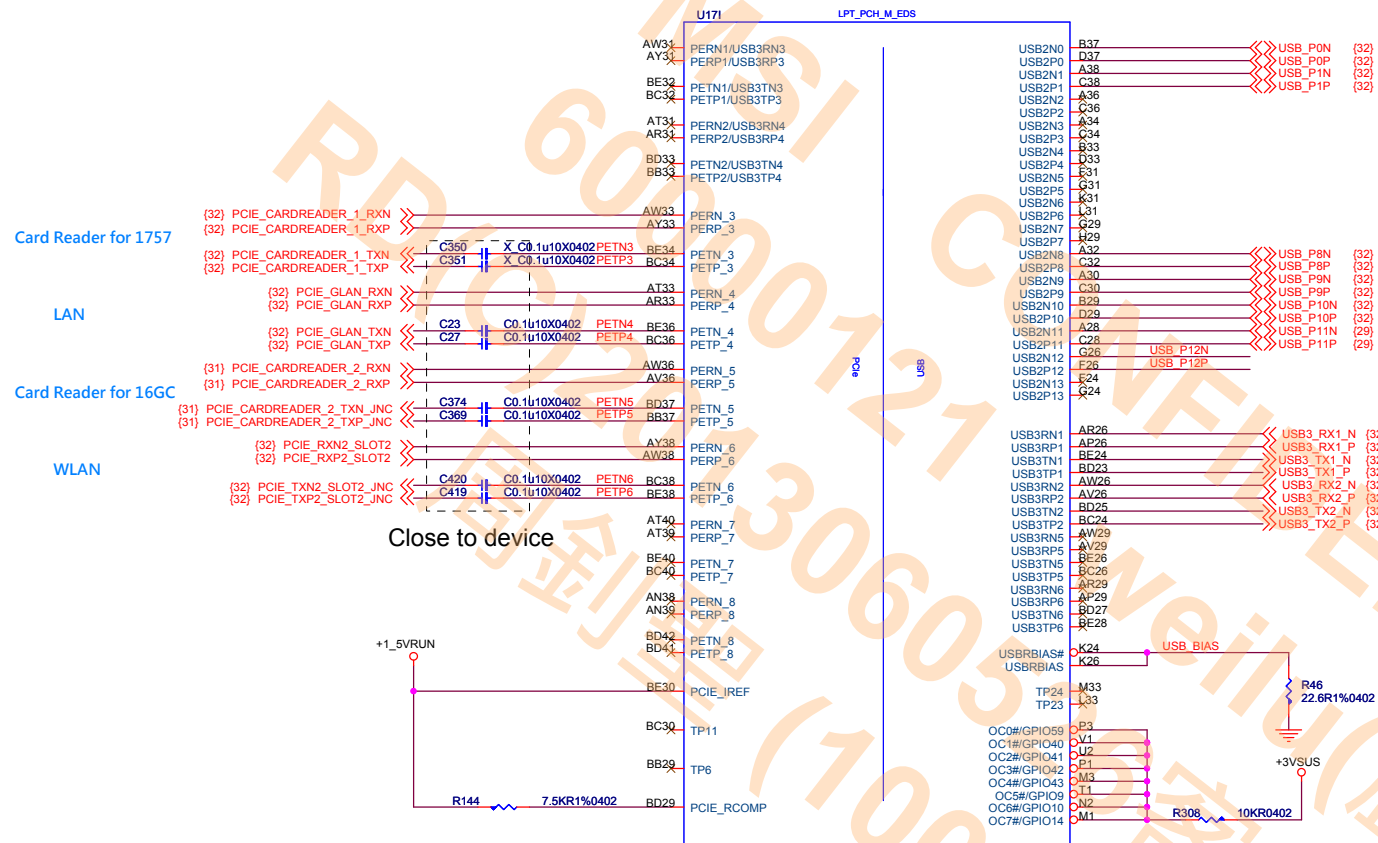
GPIO Setting : Ref 486708\_LPT\_EDS Section2.24

PLL ON DIE VR_ENABLE	
GPIO28	Internal pull high (Enable)
	Low: Disable

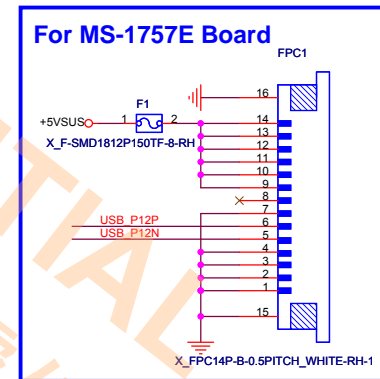


Title				PCH-6 ( GPIO,MISC )	
Size	Custom	Document Number	MS-16GC		Rev 10
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# Lynx Point ( PCIE,USB )



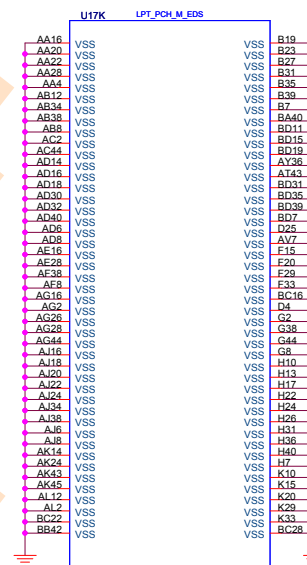
USB			
USB 2.0	USB 3.0	Device	Note
0	1	USB 3.0 Port 1	(16GCB/1757B)
1	2	USB 3.0 Port 2	(16GCB/1757B)
2			NC
3			NC
4			NC
5			NC
6			NC
7			NC
8		USB 2.0 Port	(16GCB)
9		USB 2.0 Port	(16GCA/1757A)
10		WLAN	
11		WebCam	
12		USB 2.0 Port	(1757E)
13			NC
	3		NC
	4		NC
	5		NC
	6		NC



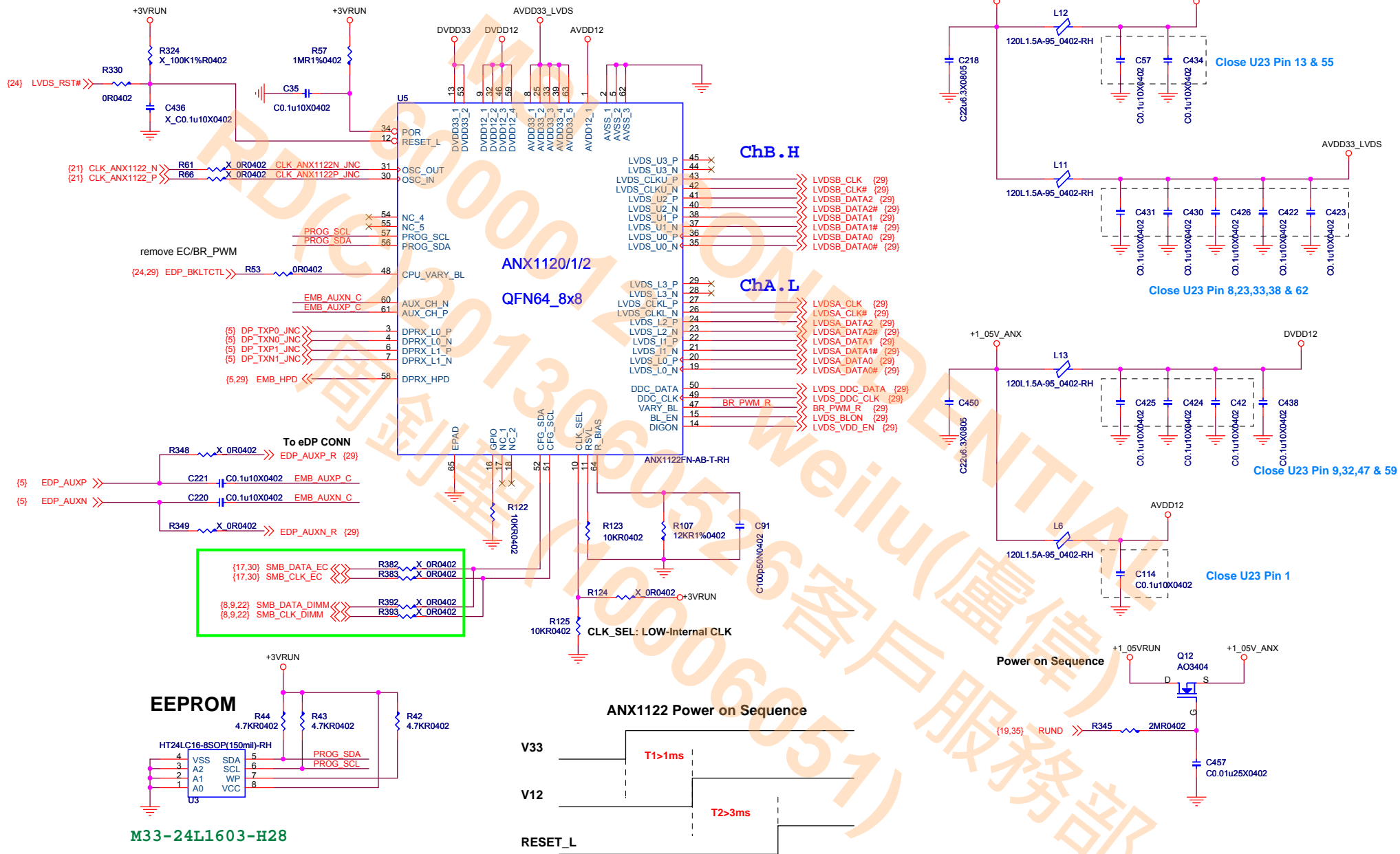
Title			
PCH-7 ( PCIE,USB )			
Size	Custom	Document Number	Rev 10
MS-16GC			
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## Lynx Point ( Power )

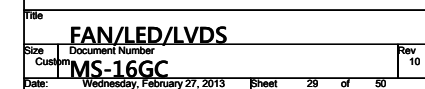


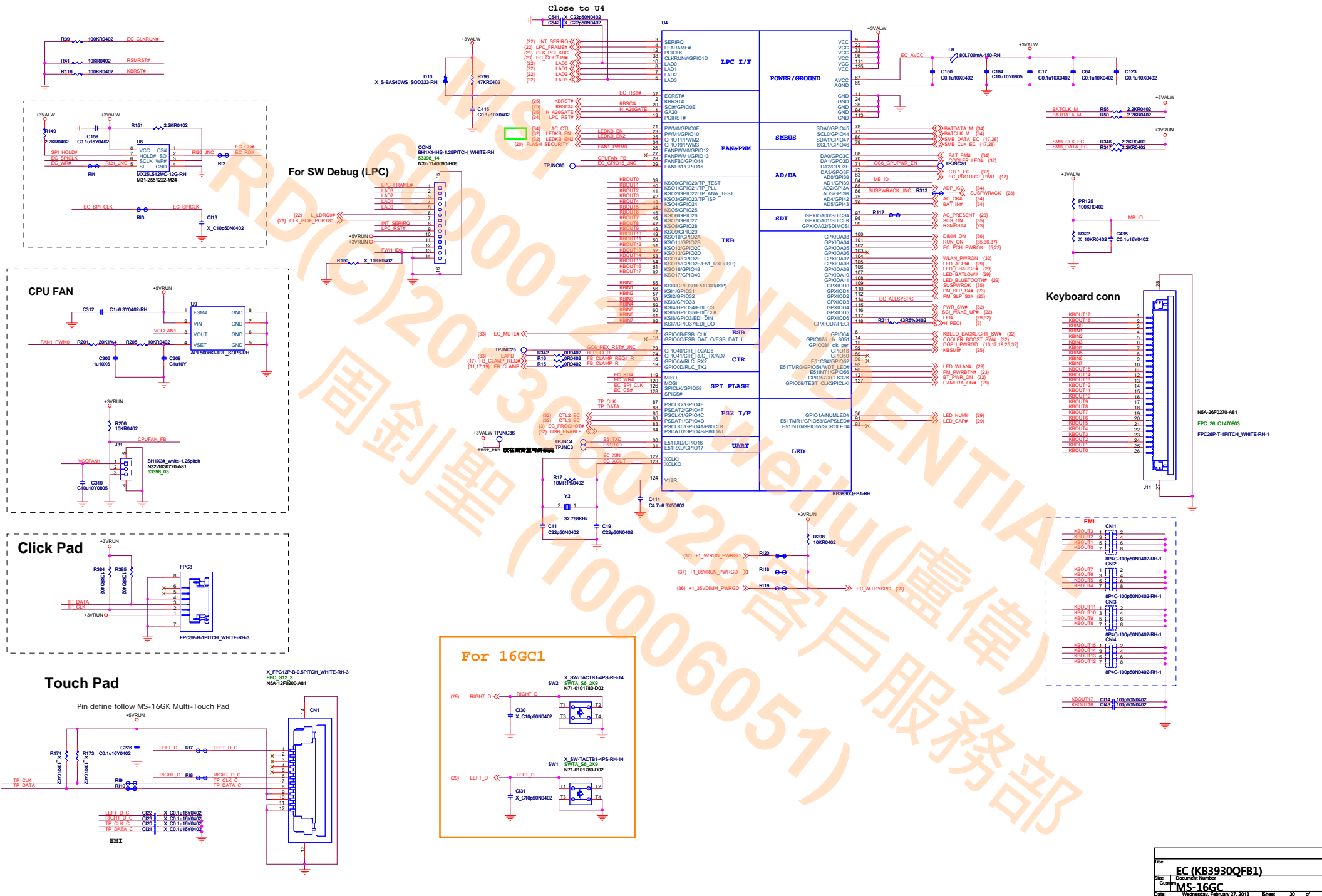
# eDP to LVDS



Title		
eDP to LVDS ( ANX1122 )		
Size	Document Number	Rev
Custom	MS-16GC	10
Date:	Wednesday, February 27, 2013	Sheet 28 of 50

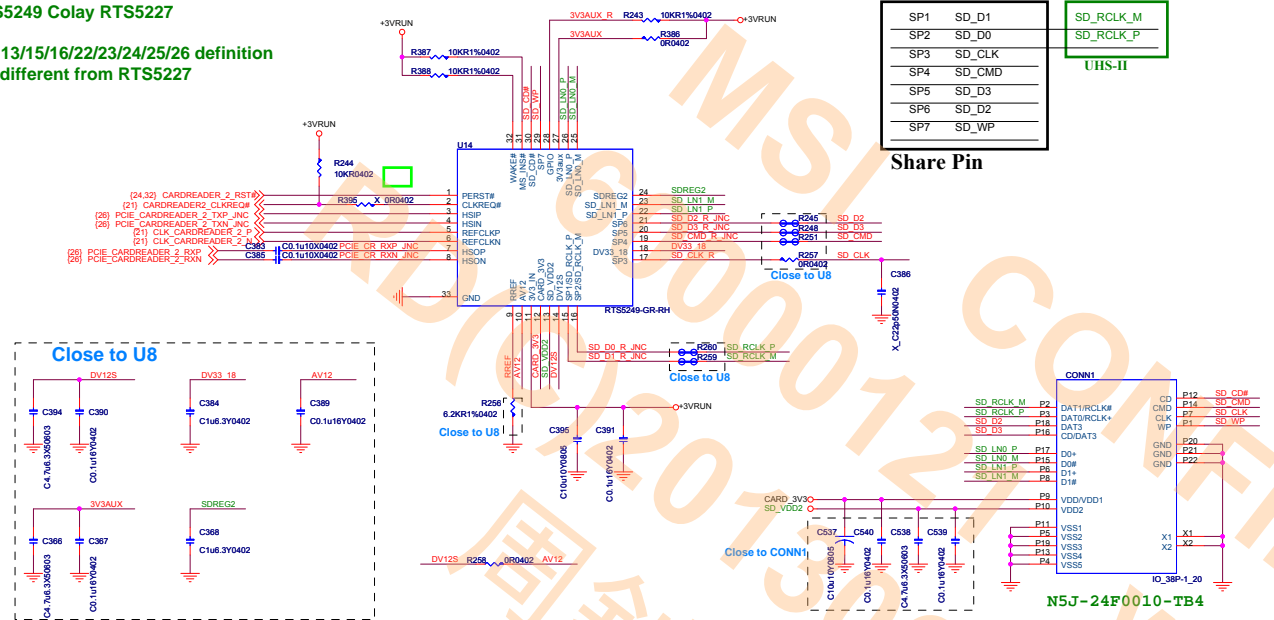
**LED**



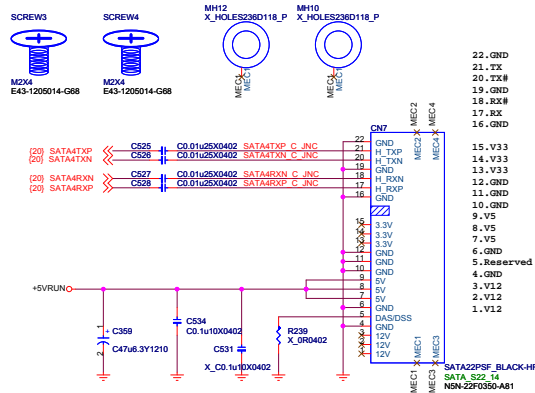


RTS5249 Colay RTS5227

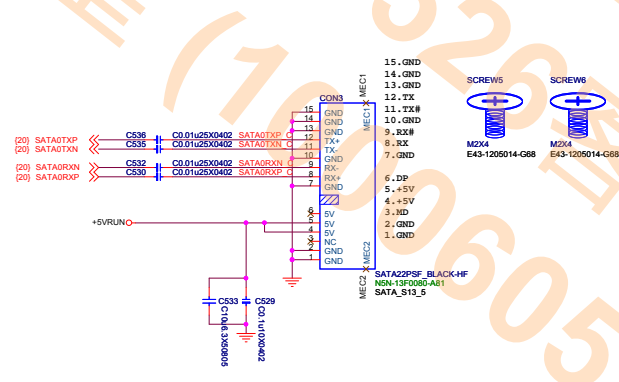
Pin 13/15/16/22/23/24/25/26 definition  
are different from RTS5227



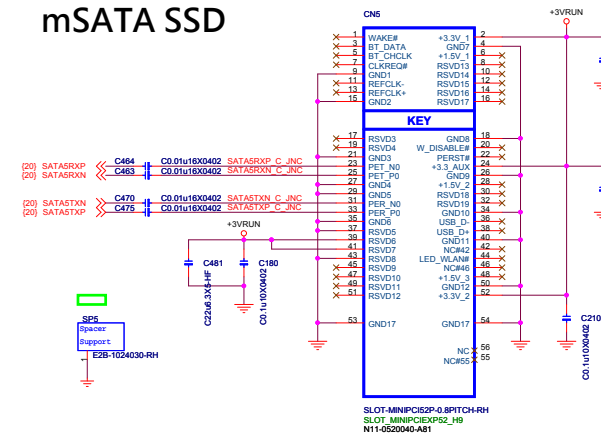
## SATA HDD



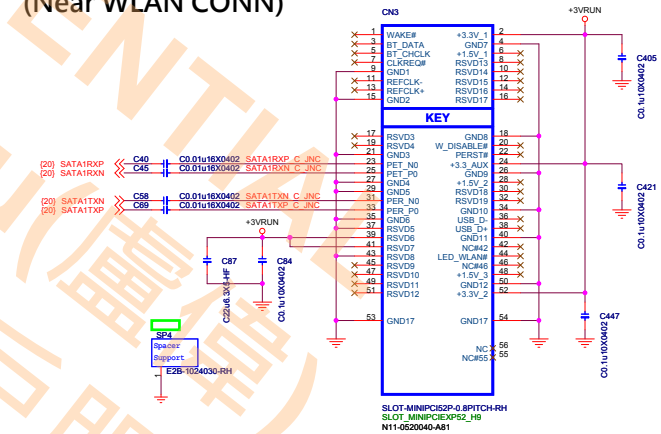
## SATA ODD



## mSATA SSD

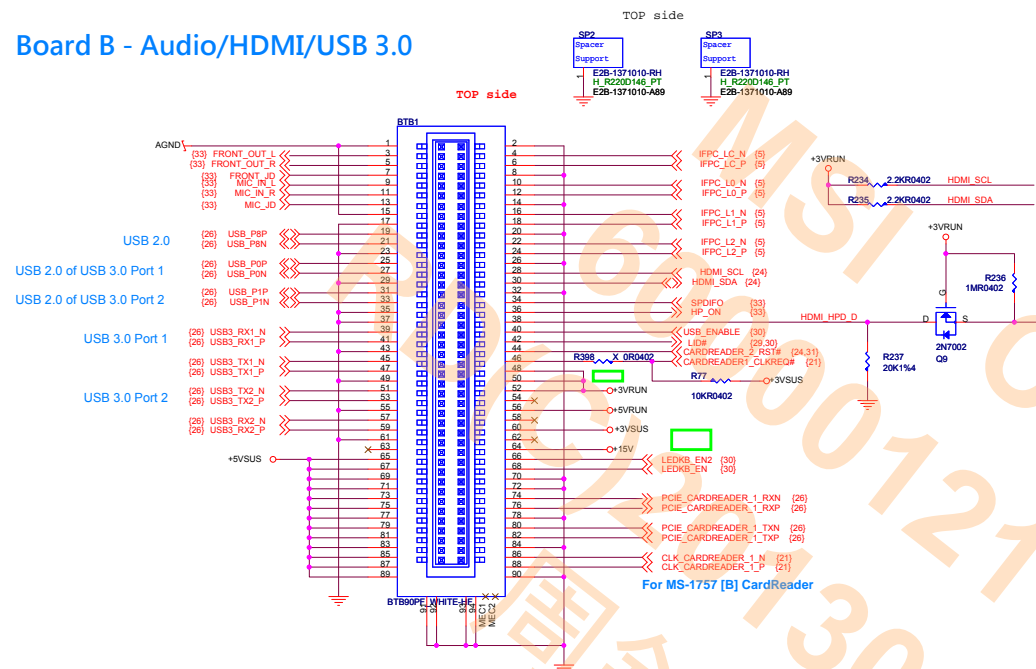


mSATA SSD  
(Near WLAN CONN)

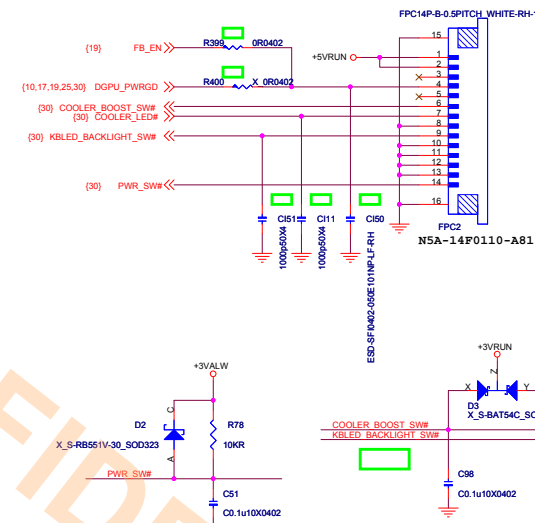




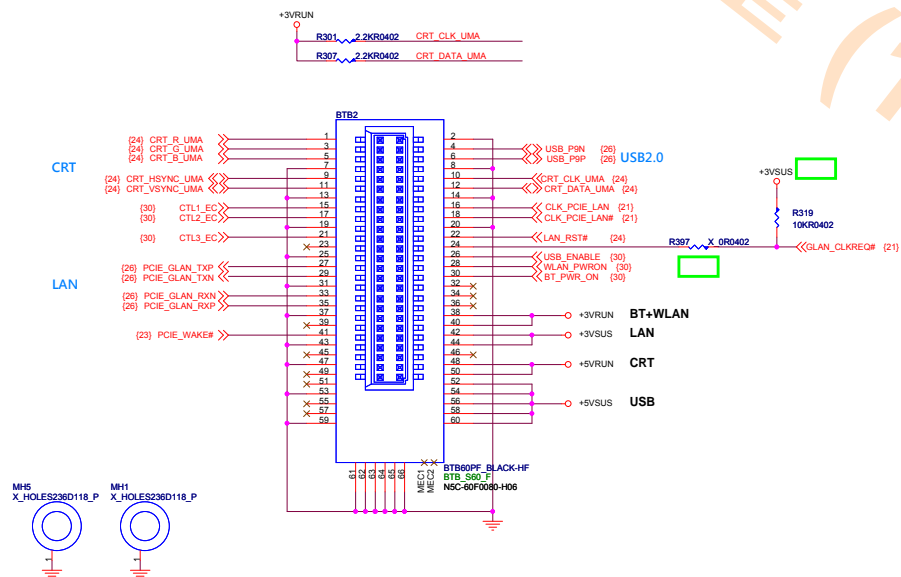
## Board B - Audio/HDMI/USB 3.0



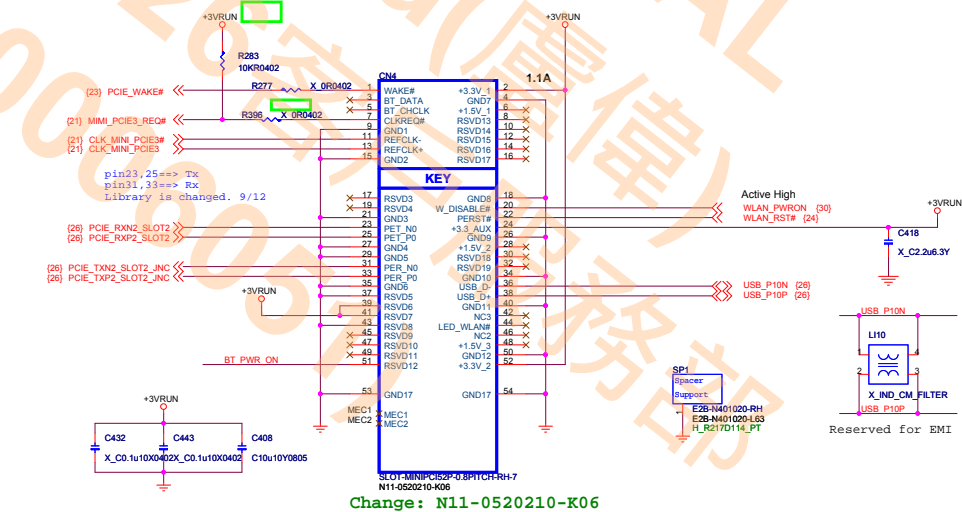
To 16GCC(Power Key Board) / FPCC1



## Board A - CRT/USB/WLAN/BT/LAN

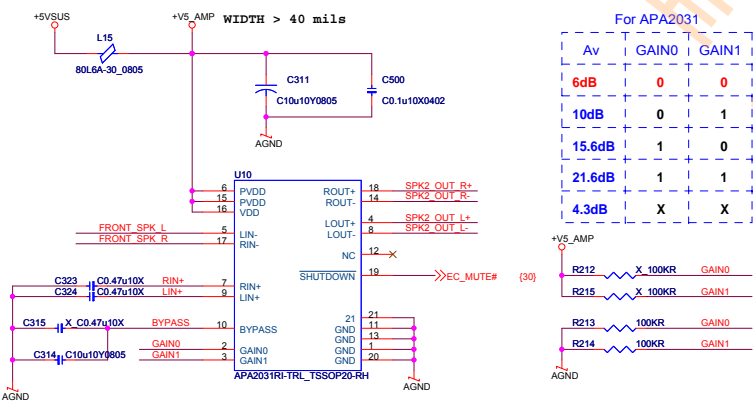
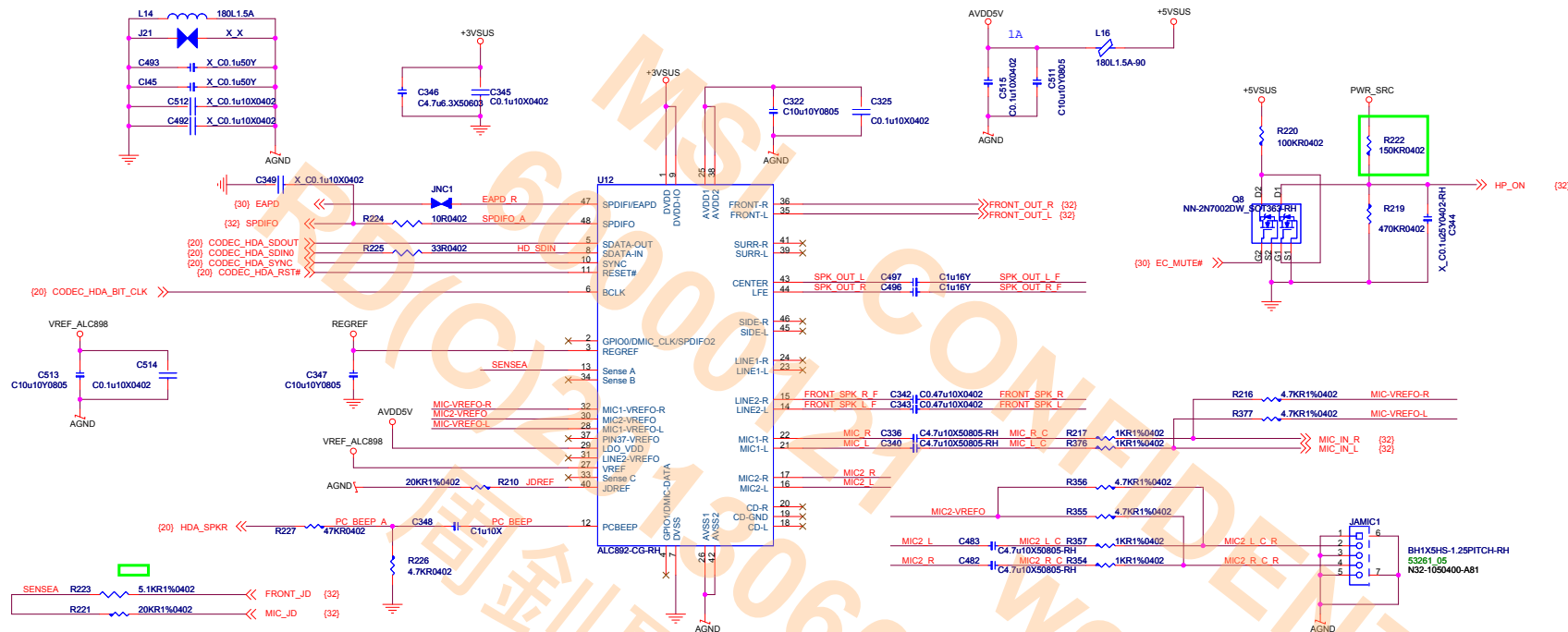


## WLAN CARD



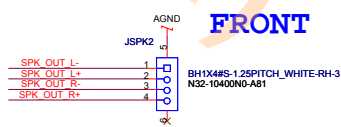
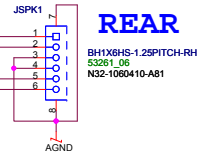
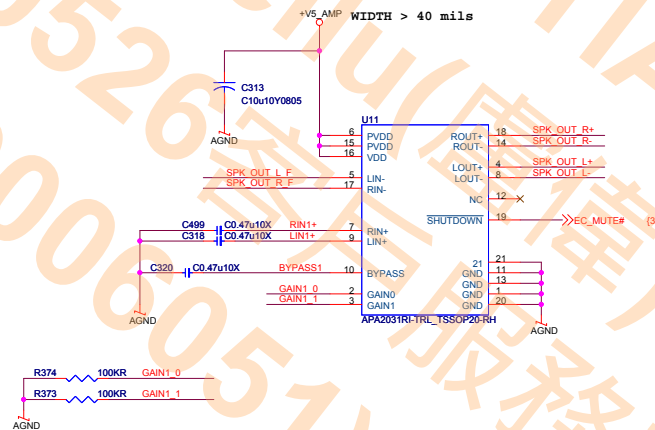
Change: N11-0520210-K06



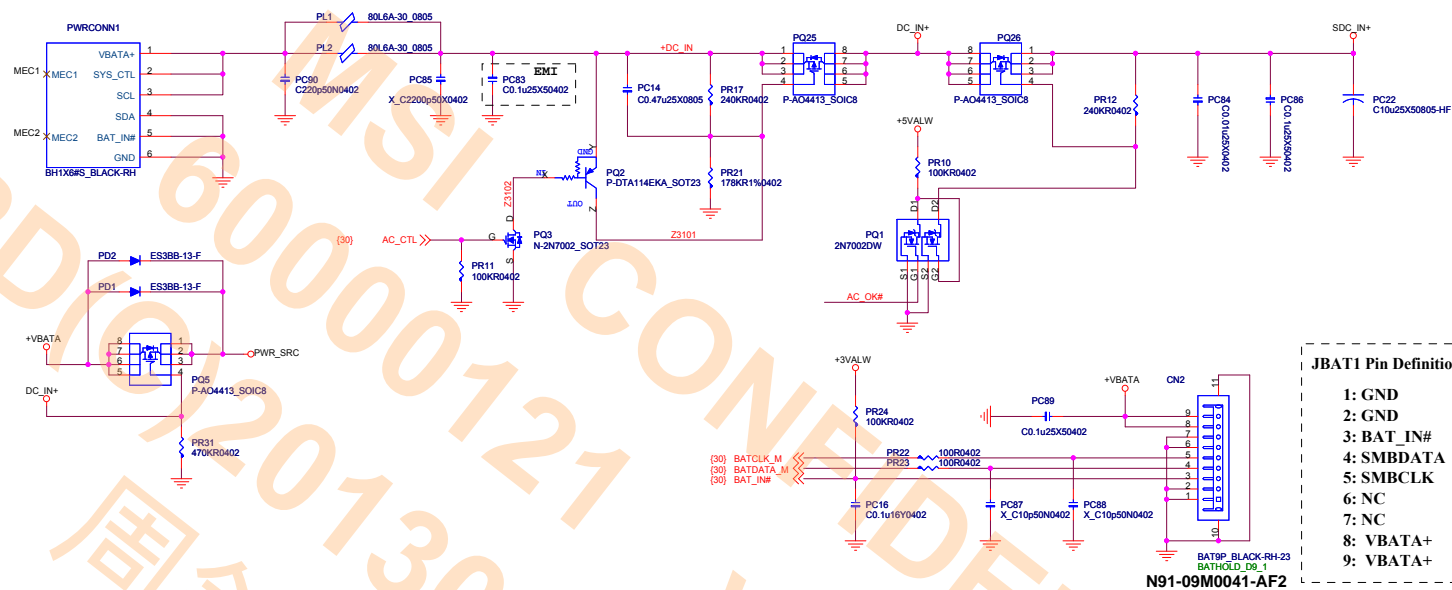


For APA2031

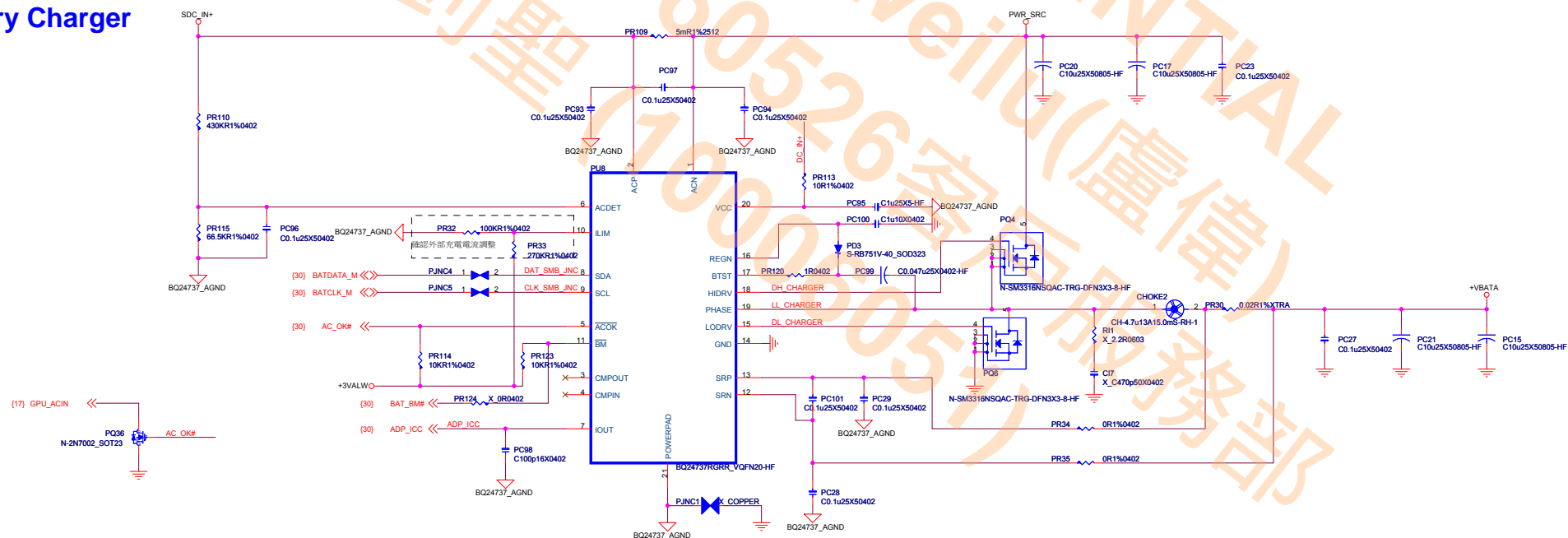
Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X



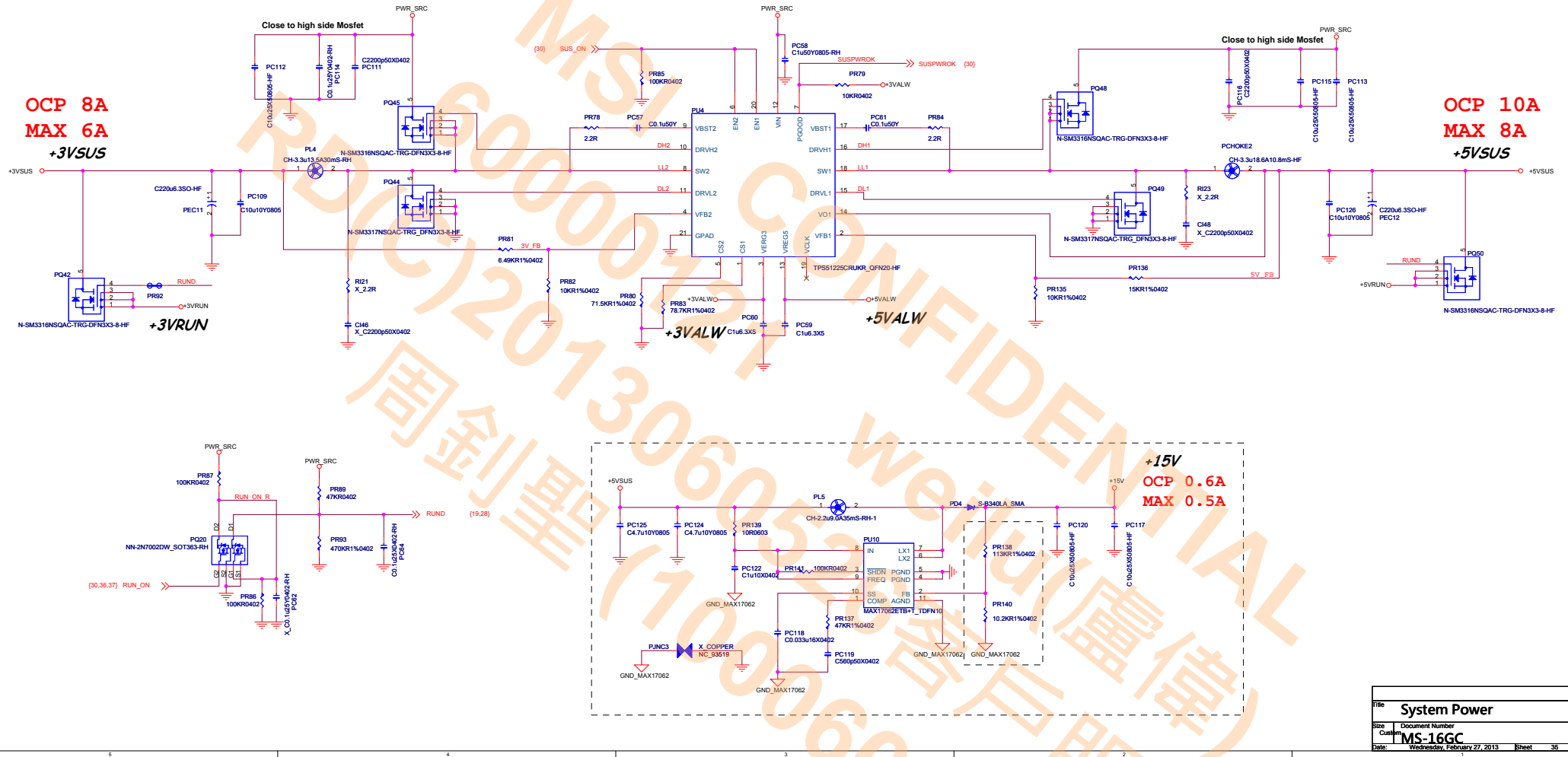
## Battery Select



## Battery Charger

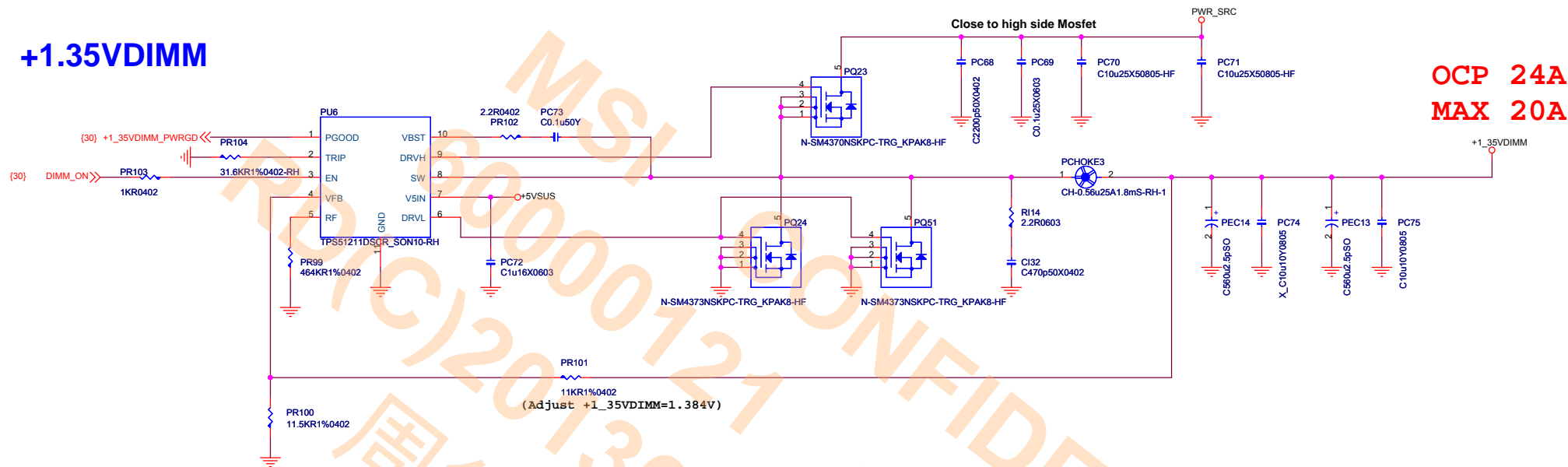


# System Power

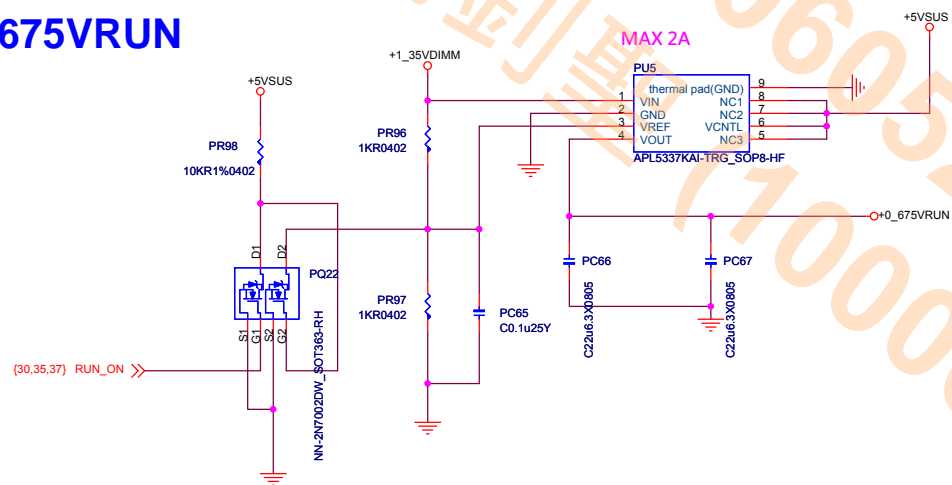


System Power		
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# +1.35VDIMM

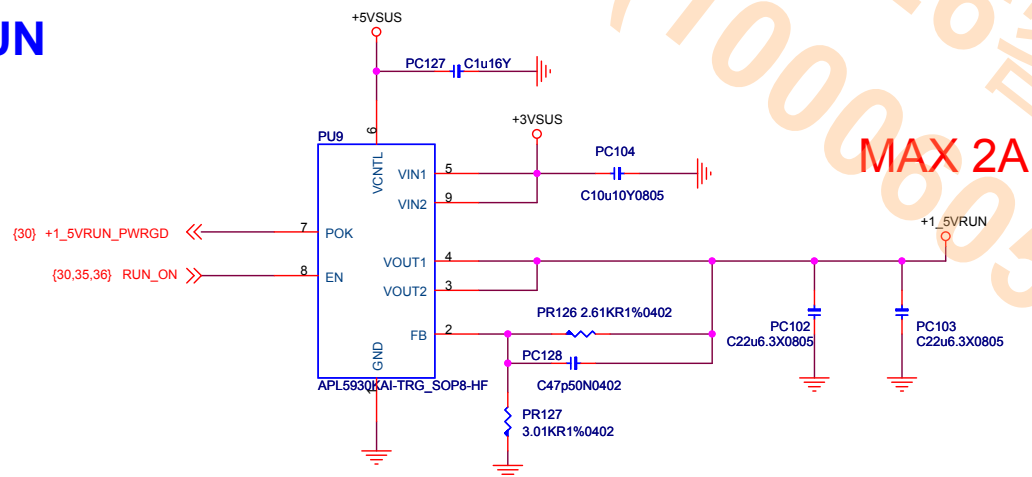


# +0.675VRUN



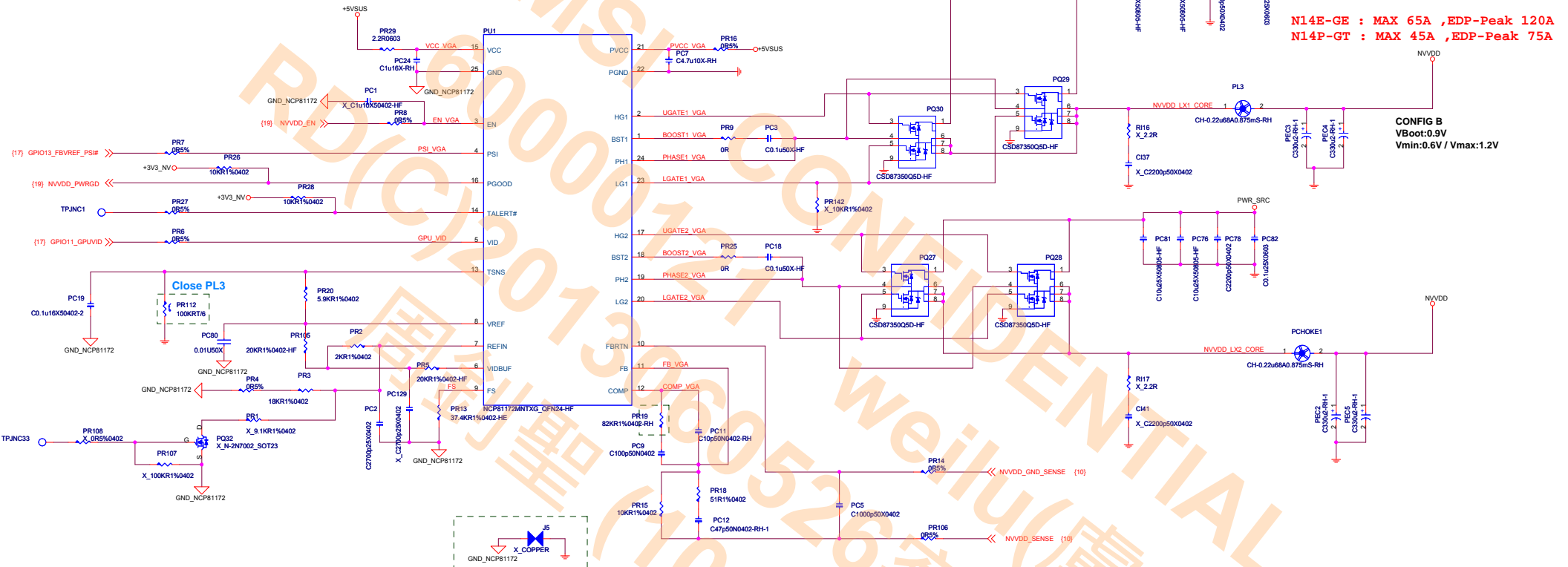
Title		+1_35VDIMM/+0_675VRUN	
Size	Document Number		
Custom	MS-16GC		
Date	Wednesday, February 27, 2013	Sheet	36 of 50
		Rev	10

## +1.5V RUN



Title				
+1 05VRUN / +1 5VRUN				
Size	Document Number			Rev
Custom	MS-16GC			10
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# DGPU POWER / NCP81172



N14E-GE : MAX 65A ,EDP-Peak 120A  
N14P-GT : MAX 45A ,EDP-Peak 75A

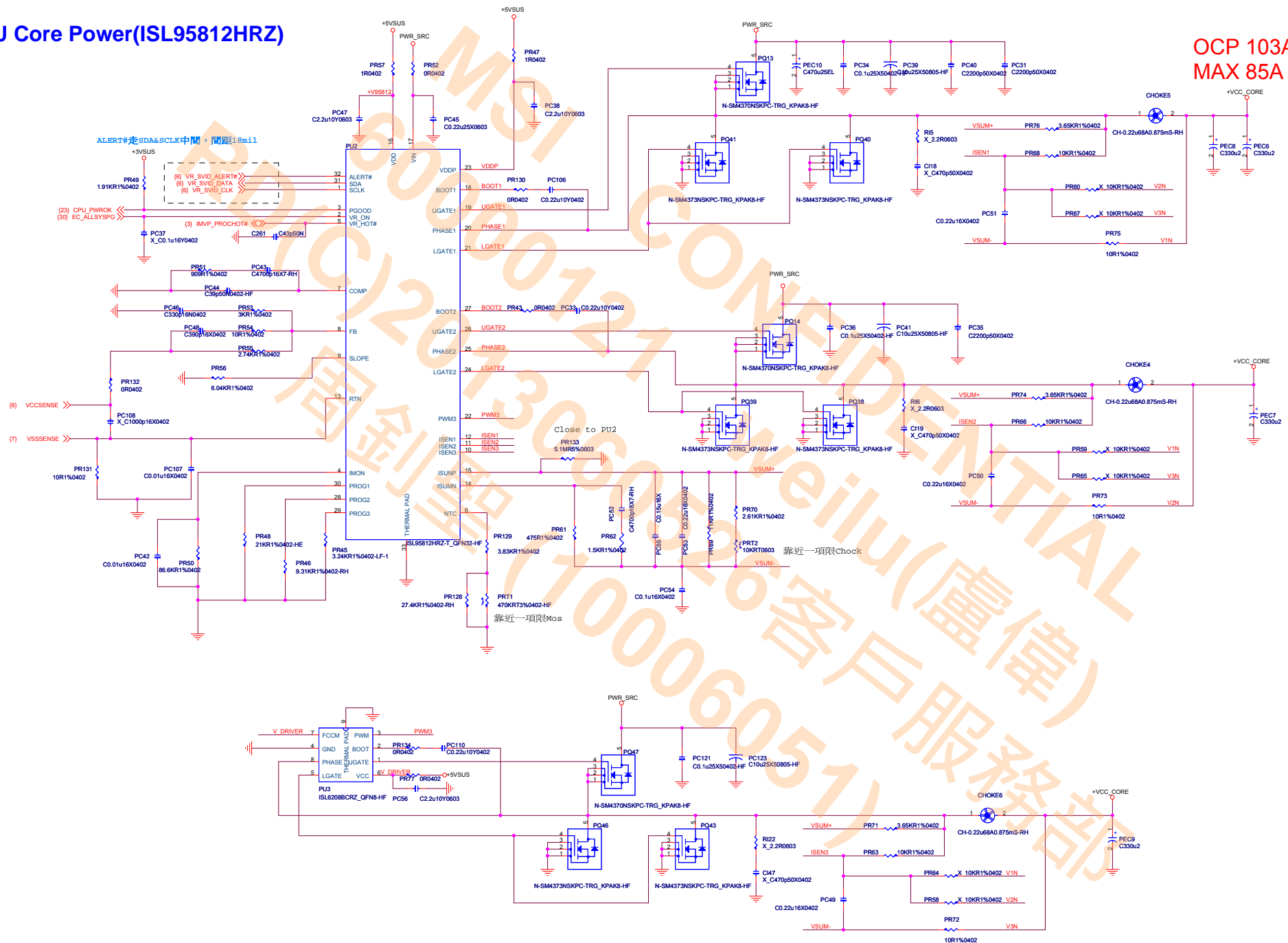
CONFIG B  
VBoot:0.9V  
Vmin:0.6V / Vmax:1.2V

File			DGPU Power
Size	Document Number	Rev	10
Custom	MS-166C		
Date:	Wednesday, February 27, 2013	Sheet	38 of 50



### CPU Core Power(ISL95812HRZ)

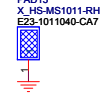
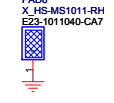
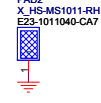
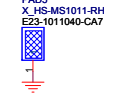
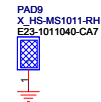
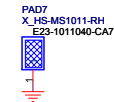
OCP 103A  
MAX 85A



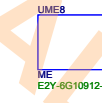
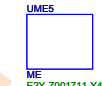
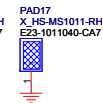
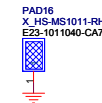
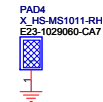
Title			
<b>CPU Power</b>			
Size	Document Number		Rev
Custom	<b>MS-16GC</b>		<b>10</b>
Date:	Wednesday, February 27, 2013	Sheet	39 of 50



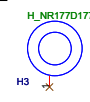
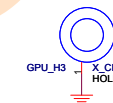
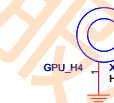
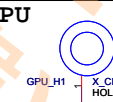
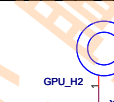
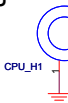
## TOP SPRING



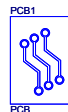
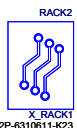
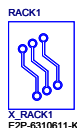
## BOT SPRING



## CPU



04/20  
ADD SB Heatsink and Screw x2



For MP: BIOS Label

Title			
Screw/ME			
Size	Document Number		Rev
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## Top Spring

PAD6  
X\_HS-MS1011-RH  
E23-1011040-CA7

PAD11  
X\_HS-MS1011-RH  
E23-5551040-CA7

PAD1  
X\_HS-MS1011-RH  
E23-5551040-CA7

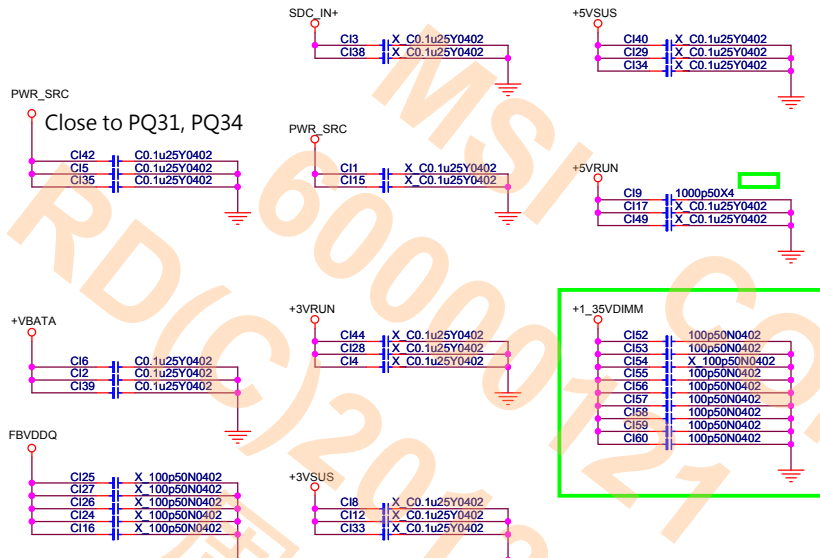
## BOT Spring

PAD12  
X\_HS-MS1011-RH  
E23-1011040-CA7

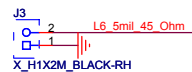
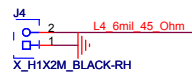
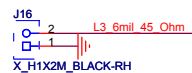
PAD15  
X\_HS-MS1011-RH  
E23-1011040-CA7

PAD3  
X\_HS-MS1011-RH  
E23-5551040-CA7

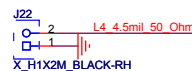
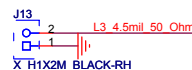
PAD10  
X\_HS-MS1011-RH  
E23-5551040-CA7



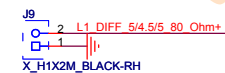
45 OHM



50 OHM



80 OHM



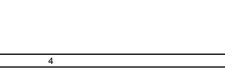
85 OHM



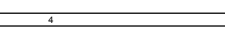
90 OHM



90 OHM



90 OHM



90 OHM



90 OHM



90 OHM



90 OHM



90 OHM



90 OHM

Title

EMI

Size Custom

Document Number

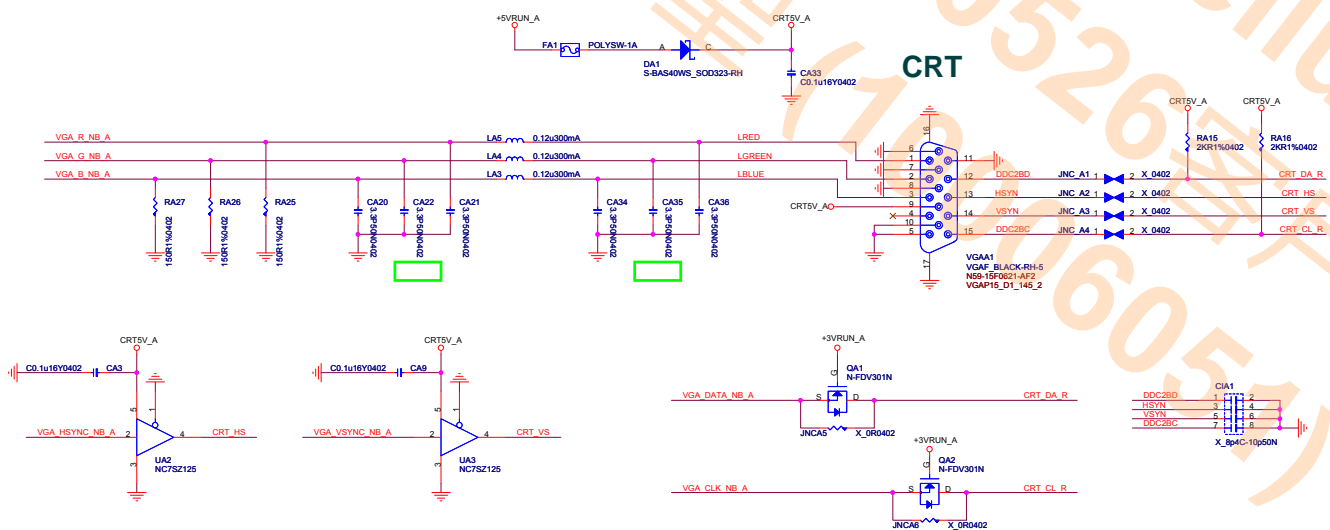
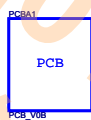
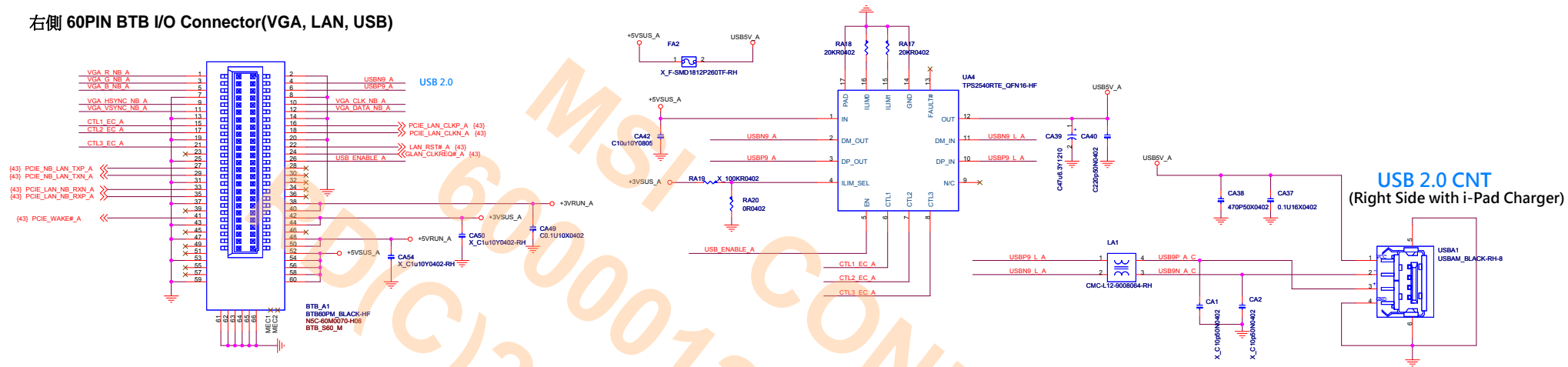
Date: Wednesday, February 27, 2013

MS-16GC

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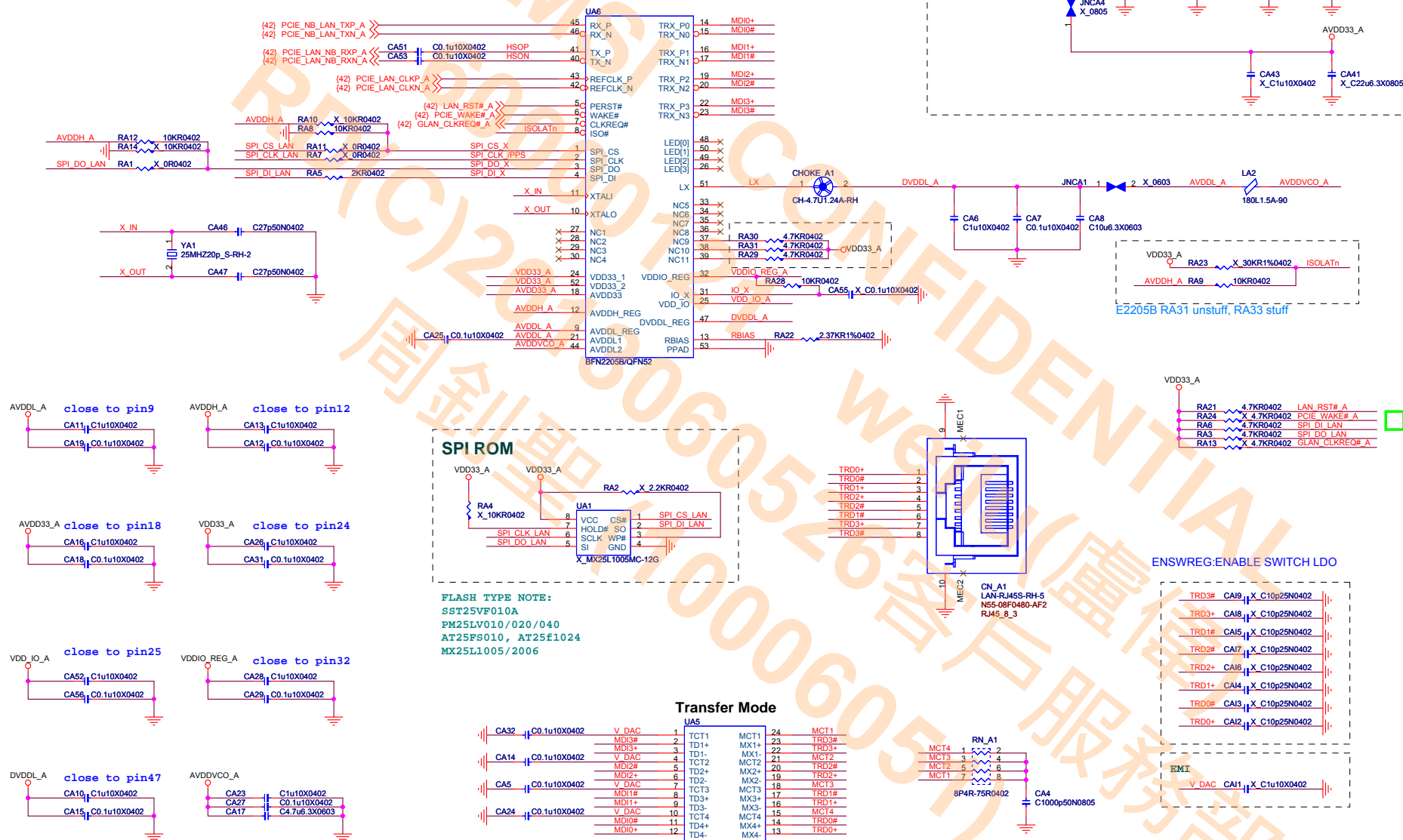
Rev 10

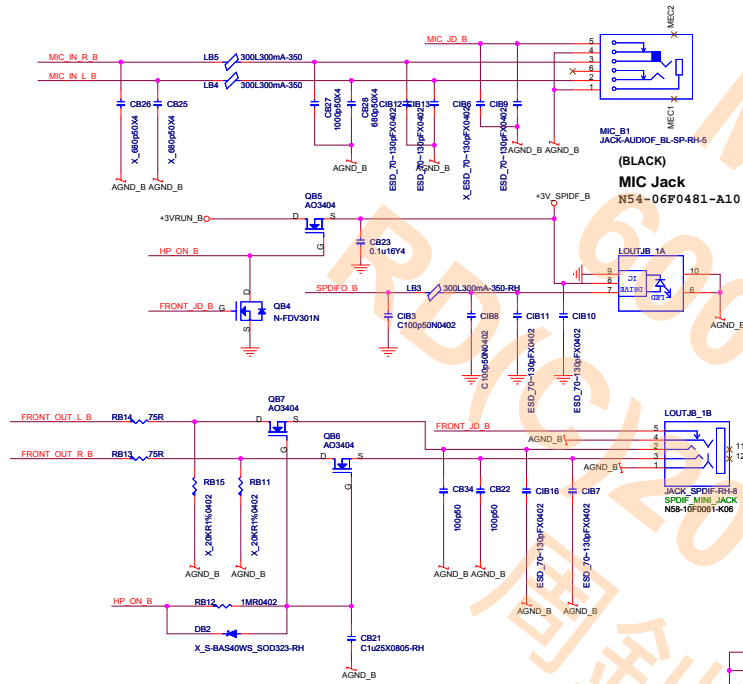
**右側 60PIN BTB I/O Connector(VGA, LAN, USB)**



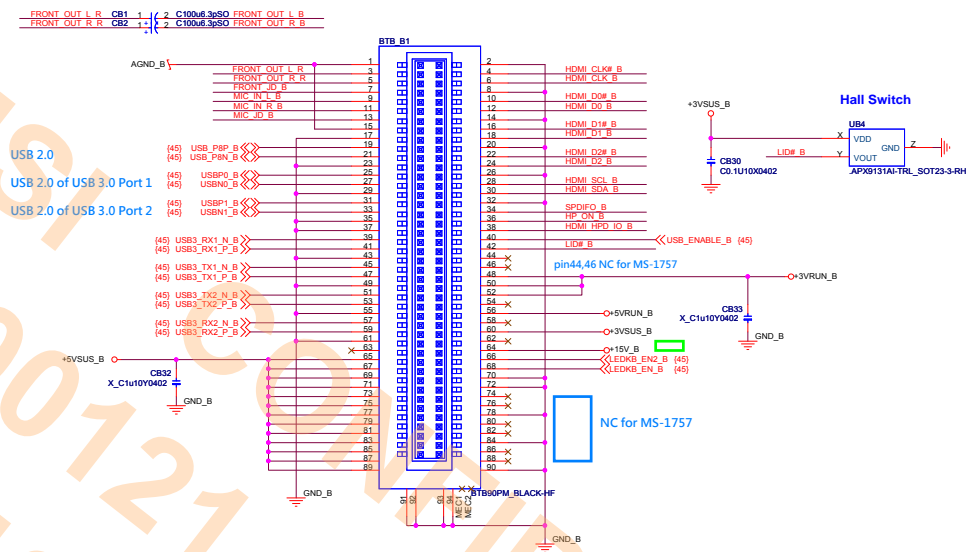
Title			
[A] BTB CNT/CRT/USB/WLAN/BT			
Size	Document Number	Rev	
Custom	MS-16GC	10	
Date:	Wednesday, February 27, 2013	Sheet	42 of 50

## GIGA LAN(BFN2200A)





## 16GCB board to board CONN1: HDMI,Audio, LED,LID

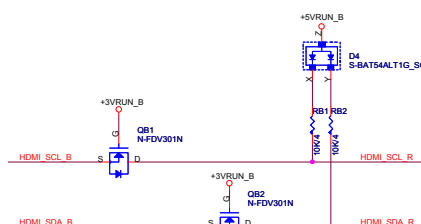
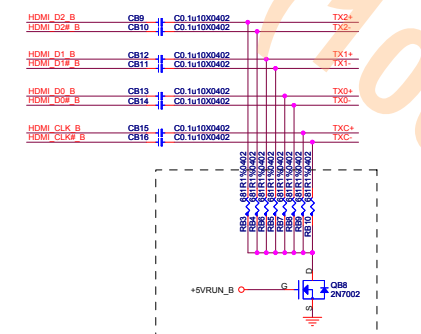
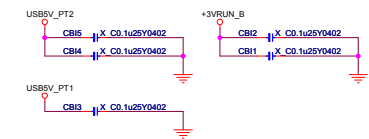


## MyIar for EMI

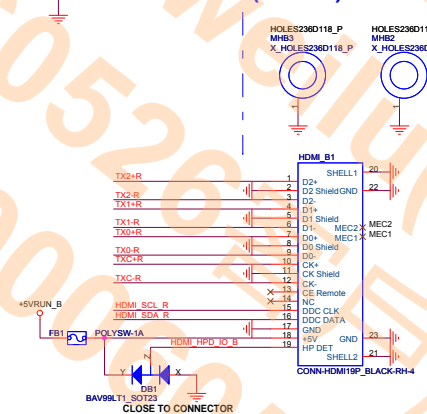


MYLAR\_B - For EMI - Audio connector 端和引脚短路 mylar  
MYLAR\_B2 - For EMI - Audio connector 端和引脚短路  
MYLAR\_B3 - For EMI - USB & HDMI Connector 端, 引脚短路 9°50mm

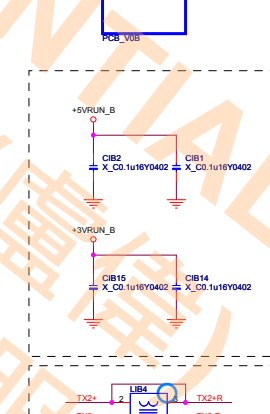
## EMI Cap



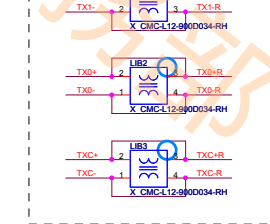
## BTB STANDOFF (16GMB)



## PCB1

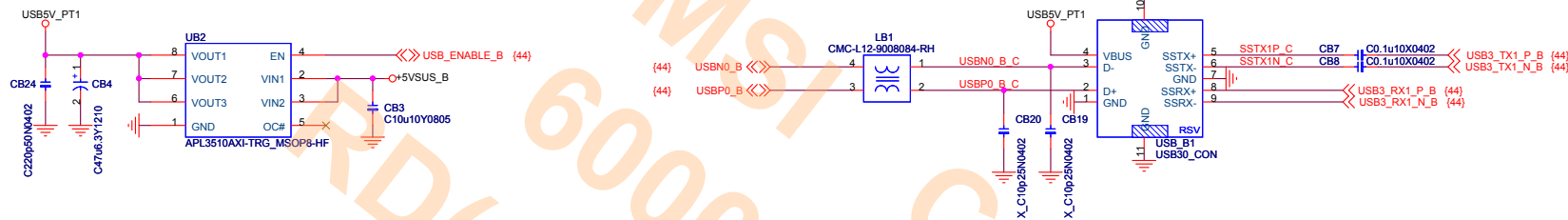


## PCB2

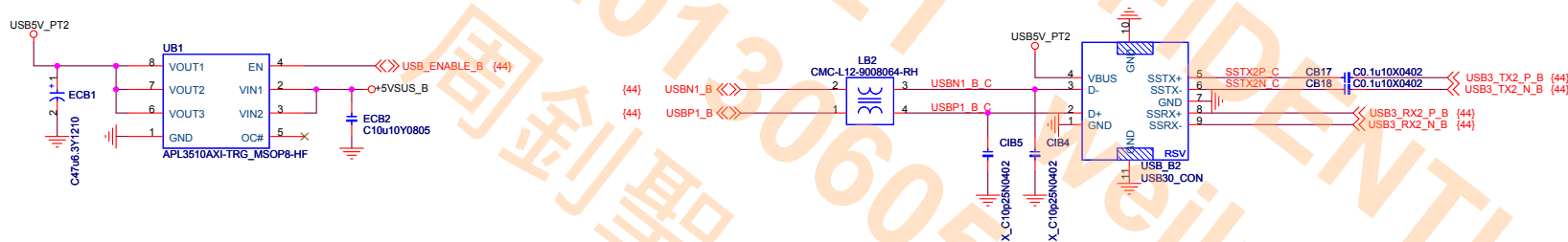




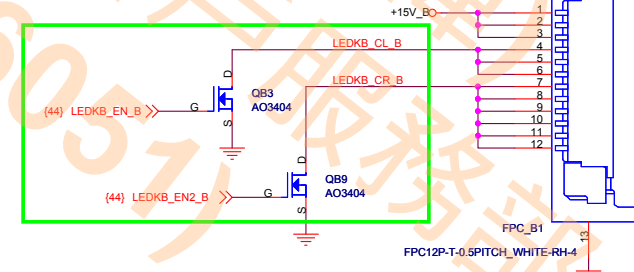
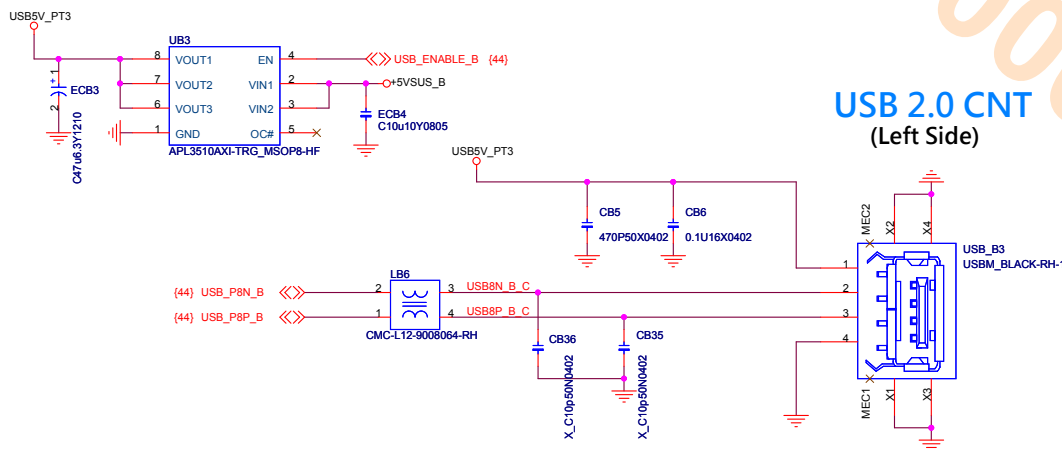
## USB 3.0 CNT1 (USB3.0 Left Side - UP)



## USB 3.0 CNT 2 (USB3.0 Left Side - Down)



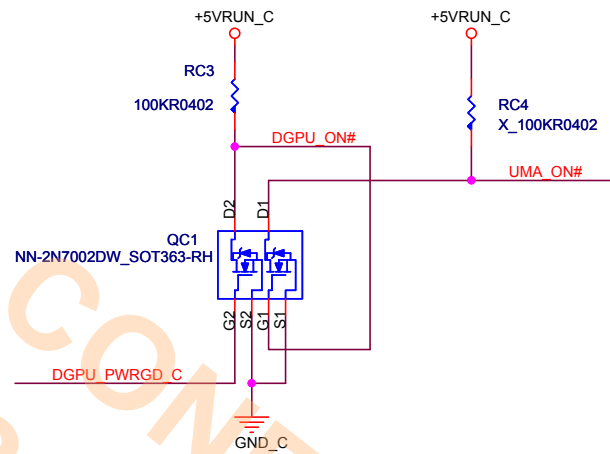
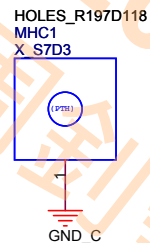
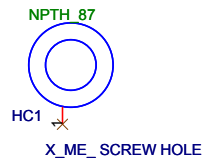
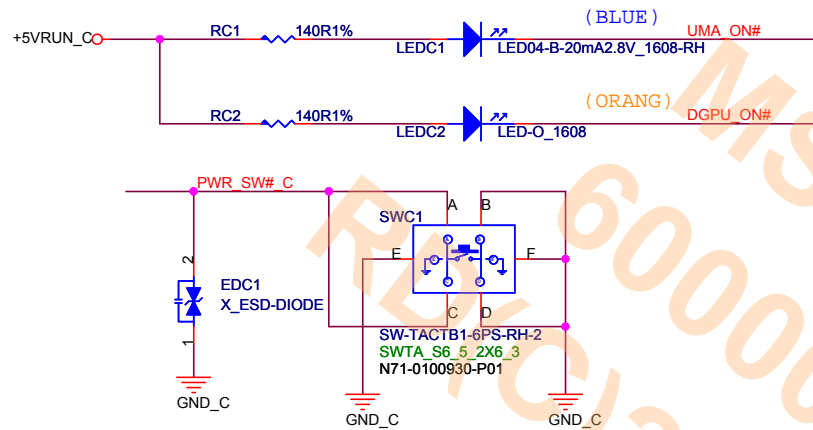
## LED Keyboard



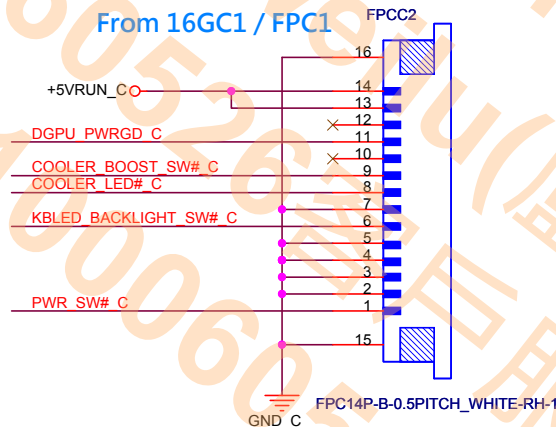
LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

N5A-12F0190-A81

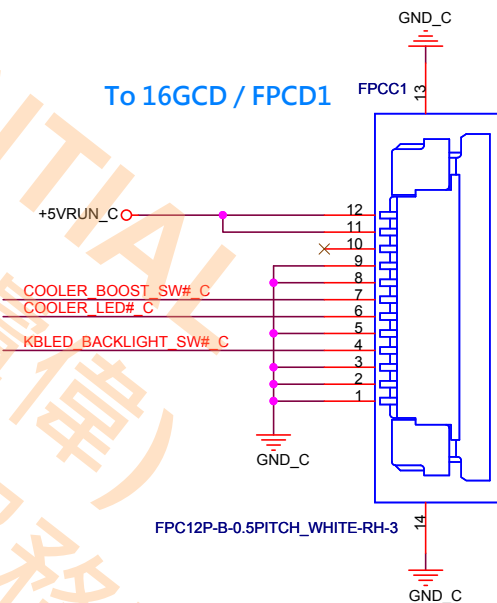
LED Forward Voltage	
R_Max	2.4V x 4 pcs = 9.6V
G_Max	3.3V x 4 pcs = 13.2V
B_Max	3.3V x 4 pcs = 13.2V



From 16GC1 / FPC1



To 16GCD / FPCD1



Title		
[C] Power SW Board		
Size	Document Number	Rev
Custom	MS-16GC	10
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+5VRUN\_D RD1 140R1% LEDD1 (BLUE) LED04-B-20mA2.8V\_1608-RH COOLER\_LED#\_D\_L

+5VRUN\_D RD2 X\_100KR0402 COOLER\_LED#\_D\_L  
COOLER\_LED#\_D QD1 2N7002 GND\_D

From 16GCC / FPCC1

+5VRUN\_D  
COOLER\_BOOST\_SW#\_D  
COOLER\_LED#\_D  
KBLED\_BACKLIGHT\_SW#\_D  
FPCD1  
FPC12P-B-0.5PITCH\_WHITE-RH-3  
GND\_D

COOLER\_BOOST\_SW#\_D  
SWD1  
SW-TACTB1-6PS-RH-2  
SWTA\_S6\_5\_2X6\_3  
N71-0100930-P01  
GND\_D

KBLED\_BACKLIGHT\_SW#\_D  
SWD2  
SW-TACTB1-6PS-RH-2  
SWTA\_S6\_5\_2X6\_3  
N71-0100930-P01  
GND\_D

COOLER\_BOOST\_SW#\_D EDD2 2 X1ESD-DIODE  
KBLED\_BACKLIGHT\_SW#\_D EDD1 2 X1ESD-DIODE  
GND\_D

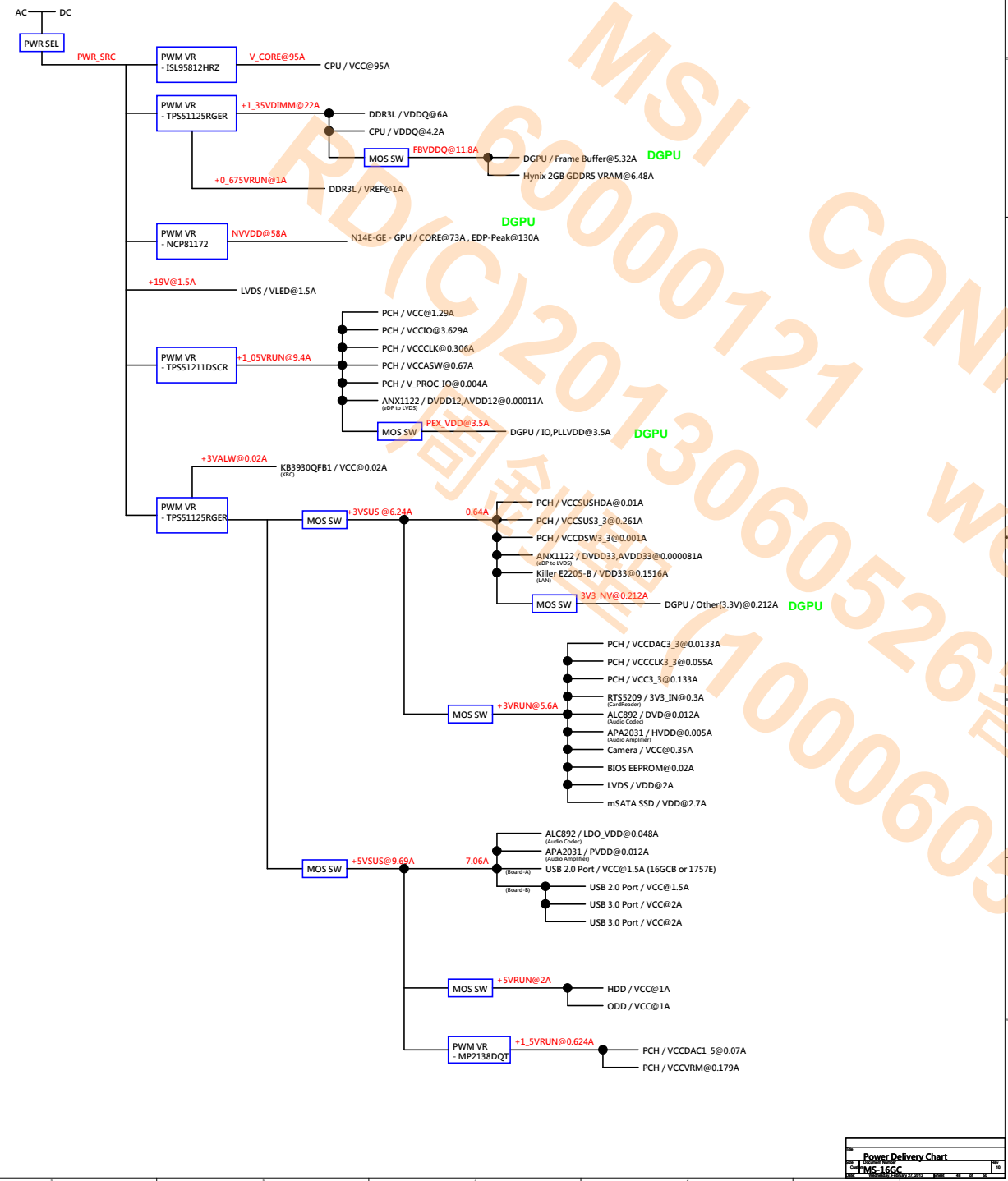
PCBD1  
PCB  
PCB\_V0B

HOLES\_R197D118  
MHD1  
X S7D3  
GND\_D

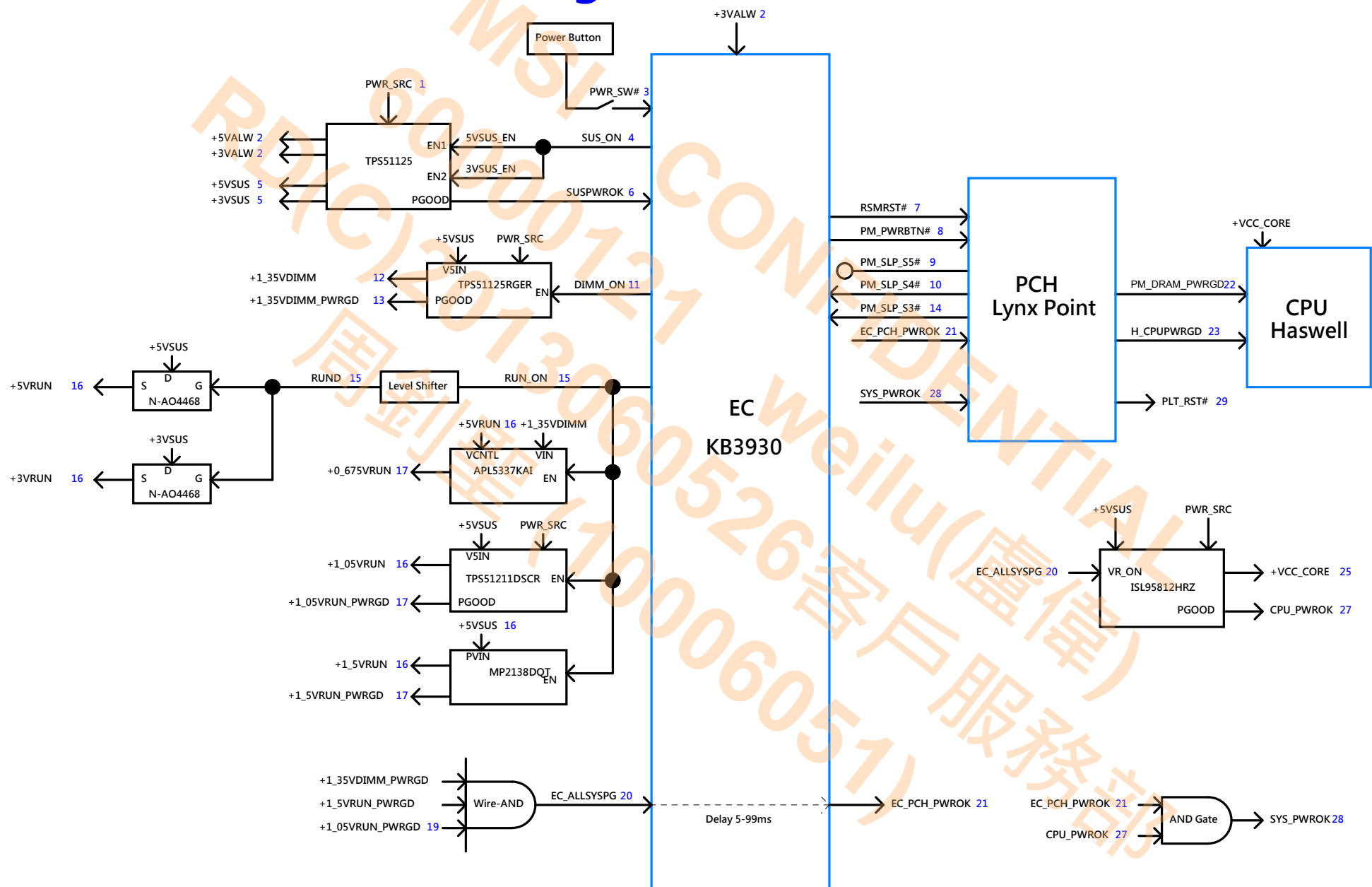
NPTH 87  
HD1  
X\_ME\_SCREW HOLE

Title			
[D] Launch Board			
Size	Document Number		Rev
Custom	MS-16GC		10
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16GC Power Delivery Chart



# 16GC Power on Block Diagram



# Power on Sequence

